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RESEARCH ARTICLE

Design of Active Fault-Tolerant Control System for Multilevel Inverters to Achieve Greater Reliability With Improved Power Quality

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ABSTRACT Modern renewable energy systems mostly utilize multilevel converter applications for improved power quality and grid synchronization purposes. A multilevel converter is an electrical device that may offer several amounts of voltage levels at the output in order to make the output more comparable to a pure sine wave. The integrity of the multilevel converter depends on the reliability of individual switches such that the converter will collapse in case of faults in these switches. In this paper, a novel 7-level Fault-Tolerant Cascaded H-Bridge Multilevel Inverter (FT-CHB-MLI) has been proposed that offers high reliability with improved power quality. A dedicated Fault Detection and Isolation (FDI) unit has been built to diagnose the faulty switch and replace it with a standby redundant switch. Total Harmonic Distortion (THD) and the determination of a normalized output voltage factor are employed for fault diagnosis. The Phase Disposition Pulse Width Modulation (PD-PWM) technique has been utilized for switching due to its superior performance as compared to other conventional techniques. This early fault detection method not only identified the issues but also performed preventative actions to keep the system healthy and stable. The proposed system was tested on the MATLAB / Simulink environment to verify its performance. The simulation results demonstrated that the THD has been reduced to almost 18% with a significant increase in reliability with advanced fault-tolerant architecture consisting of FDI units. The reliability analysis was carried out using Markov chains that also showed its increased reliability. A comparison of the proposed work with literature was also carried out to demonstrate its superior performance with increased reliability.

INDEX TERMS Fault-tolerant control, cascaded H-Bridge MLI, 7-level multilevel inverter, inverter fault diagnosis techniques.

I. INTRODUCTION

A. MULTILEVEL INVERTERS

Due to their appealing features, such as high-quality waveform and high nominal power, Multilevel Inverters (MLIs) have gained popularity among PV systems. As a result, several converters have been developed, including cascade H-bridge converters, neutral point clamped converters, and hybrid multilevel converters. These converters can be used in applications requiring medium and high power. Multilevel converters were originally used in the power train and high-voltage industrial applications. These converters were employed in utility-scale facilities for the first time in the renewable energy area, and they are still used on a wide scale in utility-scale plants today [1]–[3].

If we split single-phase multilevel converters into three categories, we get Neutral Point Clamped (NPC), Continuous Feedback (CFB), and Cascaded H-Bridge (CHB) converters. When employed in a three-level converter, the diode-clamped converter is also known as the NPC since the mid-voltage level is specified as the neutral point level [4]. The fundamental shortcoming of NPC converters in terms of the complete bridge is the requirement for dual dc-link voltage [5]. An H-bridge is a pair of capacitors and switches that produces a different input DC voltage. MLIs are used for multiple purposes in voltage going from high level to medium

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TABLE 1. Units for magnetic properties.

Component	Neutral Point Clamped	Flying Capacitor	Cascaded H-Bridge
Power Switches	12	10	12
DC Capacitors	6	0	2
Flying Capacitors	0	14	0
Clamping Diodes	16	0	0
Feed Back Diodes	12	10	12

level. Examples include their usage of magnetic levitation systems, electric traction, industrial applications, conveyors, vacuum cleaners, multiple gear systems, cooling systems, power plants, and smart houses. In multi-level inverters, stable voltage, fewer harmonics, noise, and better power factor having an improved power quality can be obtained by a small voltage step [6].

B. STRUCTURE OF A CASCADED H-BRIDGE MLI

CHB MLI has a modular structure, which is one of the reasons why so many devices have this CHB MLI. By tinkering with the power cells, we may simply increase or reduce the power level of these inverters. The H-Bridge power cells are connected in series with one another, resulting in an increase in the inverter's power and voltage level. The structure of an MLI uses four devices for switching, each of which has a diode linked in reverse to it. A DC input voltage source is linked to each power cell. A Pulse Width Modulation (PWM) output waveform will be generated by these power cells. The waveform will be in the shape of stairs. The Cascaded H-bride inverter is divided into 2 types [7]. They are:

1) Asymmetrical Cascaded H-Bridge MLI
2) Symmetrical Cascaded H-Bridge MLI

The input DC source is the basis for this division. An inverter is called a Symmetrical CHB inverter if it has equal valued DC voltage sources. In asymmetrical CHBMLI, unequal DC voltage sources are used. Table 1 examines a variety of devices and their reliability, as well as MLI mechanisms at all seven levels.

A total of (n - 1) × 2 power devices used for switching and (n - 1)/2 multiple DC sources are needed for an n-level cascaded H-Bridge Multi-Level Inverter. The first cell's output voltage can be calculated as follows:

$$V_{CX1} = (S_1 - S_2) \times E_{dc} \tag{1}$$

where

E_{dc} = DC voltage source

V_{CX1} = Output voltage of the first power cell

$S_1 \& S_2$ = Switches SW1 and SW2 for switching functions

Additionally, add up to stage for M number of cells to calculate the desired output voltage associated with the arrangement as follows:

$$E_{OX} = V_{CX1} + V_{CX2} + V_{CX3} + \cdots + V_{CXM} \tag{2}$$

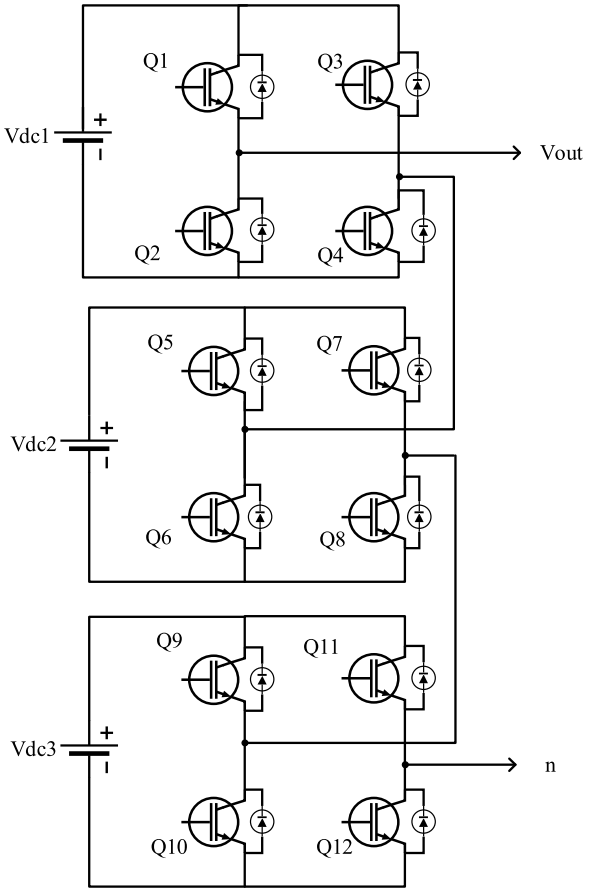

FIGURE 1. Schematic diagram of 7 levels cascaded H-Bridge multi-level inverter.

The schematic of seven levels multi-level inverter is shown in Figure 1.

Here each bridge will produce the output of three stages. One is + Vdc, the second is 0 and the third is −Vdc. When the bridges are cascaded, a staircase waveform of seven levels is produced giving us our desired result. The CHB topology is mostly used for multilevel inverters due to the following advantages:

1. There are more than twice as many potential output voltage levels "m" as there are dc sources "s" (m = 2s + 1).

2. The H-bridge series allows for flexible modular architecture and packaging. This will allow for a faster and more cost-effective production procedure.

C. FAULT-TOLERANT CONTROL

Fault-Tolerant Control (FTC) techniques are used to increase machine dependability by avoiding occurrences that cause failure due to faults. A fault is defined as a variation in a system's output from its planned output, whereas a failure is defined as a full shutdown of a system. An FTC's primary function is to avoid malfunctions in important systems that might lead to their failure. Systems utilized for essential tasks,

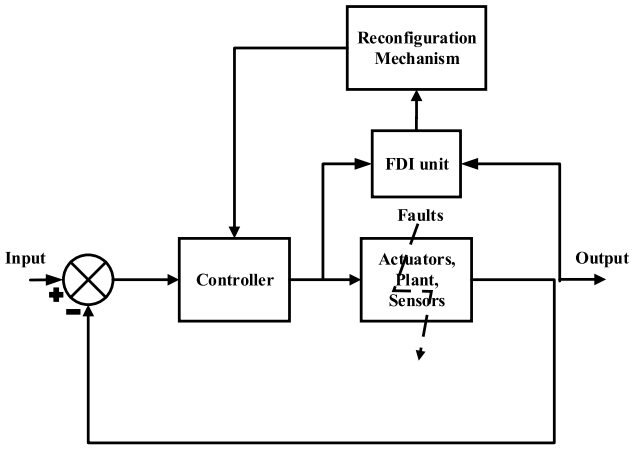

FIGURE 2. AFTCS Architecture [10].

such as unmanned aerial vehicles, planes, and nuclear power plants, cannot tolerate failure; hence, FTC is employed to increase the safety and dependability of such systems. [8]

One of the most significant components of the solar system's consistent functioning is the inverter's dependability. The advantages of a multi-level converter include reduced harmonic content in the output voltage, lower switching loss, and lower stress, making it the optimum choice for medium-high voltage and high power applications. However, because of the increased number of power switching devices, the multi-level inverter would raise the risk of a defect, lowering the system's dependability. Once the multi-level inverter fails, it will result in massive economic losses or catastrophic accidents. As a result, increasing the dependability of multilayer inverter systems is critical.

One of the strategies used to construct an FTC system is redundancy, which is divided into two categories: analytical redundancy and hardware redundancy. Active and passive analytical redundancy are the two types of redundancy. The active analytical redundancy comprises fault detection, isolation, and controller reconfiguration, but it is complicated, computationally intensive, and sluggish in performance; yet, it has the benefit of embracing a wide variety of defects. Because it is based on a strong controller design that can deal with the only considered uncertainties and faults in a system, passive analytical redundancy is a relatively simple and quick technique. However, it cannot handle a wide variety of defects [9].

The Fault Detection and Isolation (FDI) unit is the most important part of an Active Fault-Tolerant Control System (AFTCS), and it is responsible for detecting problems in actuators and sensors, as shown in Figure 2. The FDI unit is created by creating an observer model that creates estimated values that are utilized in the event of a component failure. The FDI performs controller reconfiguration after recognizing and isolating a malfunction by employing the estimated parameter values by the observer to adopt new circumstances. AFTCS has the benefit of supporting a wide range of defects and being an online fault detection-based system, but it is also complicated, computationally intensive, and slow to perform [10].

II. LITERATURE REVIEW

The authors in [10] focused on the principles of FTC and the application of artificial intelligence in FTC systems. FDI and fault monitoring solutions have been developed to handle many types of control system defects and errors [11]. A switch-dependent control system for running an inverter is presented when one or more switches are disabled. In Fault Mode, just the faulty devices are utilized to drive an inverter, while the control signals for the remaining devices in a disturbed cell are modified according to the kind of fault [12].

A defect detection and reconfiguration approach has been developed for CHB 11-level inverter drives. The developed fault diagnosis paradigm has been validated, and the system's stability may be enhanced [13]. A hybrid system for ''Hybrid Renewable Energy Sources (HRES)'' has been proposed in [14] which includes a ''solar-wind power generation'' platform with nine-level, thirteen-level, and seventeen-level inverter designs with an updated MLI architecture. The disadvantage of the suggested topology is that if one of the H-bridges breaks, the MLI will still function with a decreased number of levels. The load, on the other hand, cannot get full power [15].

A fault detection system and tolerance regulation have been suggested for a single-phase CHB MLI. Since the existing flow direction for open-fault and short-fault is different, the CHBMLI requires safety fuses to distinguish between the two [16]. A control technique for a single-phase cascaded ''off-grid'' solar panel storage system has been presented, as well as a fault-tolerant system in the event of PV failure. When PVs crash, several operating modes, such as normal mode, 50% fault mode, and 100% fault mode, are strongly considered to increase device stability, depending on their states [8]. Hybrid modulation is used to reduce switching errors. The suggested regulation for fault-tolerant systems thus ensures dependable power generation by managing different types of converter cells separately. The semiconductor switches used in H-bridges determine their stability. Faults in these parts can cause the device to stop working completely.

In the paper [17], the authors describe a fault-tolerant system with dual redundancy and an FDI device that can locate and replace a defective device with standby in order to prevent the system from shutting down unexpectedly and to maintain operation stability, thereby improving reliability. A fault-tolerant H-bridge with dual redundancy and an FDI unit is shown to be a very efficient solution for DC motor speed modulation in this study.

The CHB converters may be connected to the Medium Voltage (MV) grid stations for installation. The point is because transformers have high power and low harmonics, we can accomplish it without them. They're crucial for linking large-scale renewable energy installations to the power grid. In a grid-connected CHB converter, on the other hand, the number of power switching devices can have a substantial

influence on its efficiency. The study [18] suggests a methodology based on two zero-sequence voltage injection methods and DC voltage optimization to improve the efficiency of Y-linked CHB converters when one or more module units are bypassed. Using an extension theory-based assessment method, the research proposes a method for diagnosing defects in inverter-driven motor driving systems. A three-level NPC inverter is initially created to check and diagnose defects in NPC inverters. The Fast Fourier transformation (FFT) is used to convert the signals of an I (line), i.e. current through the line, from the time domain into a broad range of frequency domain in order to perform a fault analysis with multiple power transistors on the related continuum of characteristics of an inverter. The sorts of faults, links, and coordination in a specific region are then identified as aspects of a thorough review process [19].

The paper [20] describes a defect detection transition control strategy based on a predictive model. An asymmetric zero voltage situation is required for an open-circuit problem diagnosis. The authors suggest a simpler approach that is based on zero-voltage switching and has been tested for both non-linear and linear loads. The authors offer a strategy for identifying short circuit defects based on an output voltage compared to the reference voltage of CHB MLIs with five levels (a neural network for a five-level CHB). A network-based technique to defect detection is adopted. The authors in [21] propose the use of MLIs to determine the kind of problem and its location, including five MLIs with several layers. The authors of [22] noted how, while MLIs have enticing properties, their large range of applications is constrained by the standard setup's usage of additional switches. With the fewest amount of unidirectional switches and gate trigger circuits, an elaboration on the contemporary 7-level MLI architecture is achieved, resulting in the lowest switching failures, as well as a smaller size and cheaper installation cost [23].

In this paper, a novel 7-level Fault-Tolerant Cascaded H-Bridge Multilevel Inverter (FT-CHB-MLI) has been proposed that offers high reliability with improved power quality. A dedicated FDI unit has been built to diagnose the faulty switch and replace it with a standby redundant switch. Total harmonic distortion and the determination of a normalized output voltage factor are employed for fault diagnosis. The Phase Disposition Pulse Width Modulation (PD-PWM) technique has been utilized for switching due to its superior performance as compared to other conventional techniques. This early fault detection method not only identified the issues but also performed preventative actions to keep the system healthy and stable. The proposed system was experimentally tested on the MATLAB / Simulink environment to verify its performance. The simulation results demonstrated that the Total Harmonic Distortion (THD) has been reduced to almost 18% with a significant increase in reliability with advanced fault-tolerant architecture consisting of FDI units. The reliability analysis was carried out using Markov chains that also showed its increased reliability. A comparison of the proposed work with literature also depicted its superior performance in achieving its superior power quality and increased reliability.

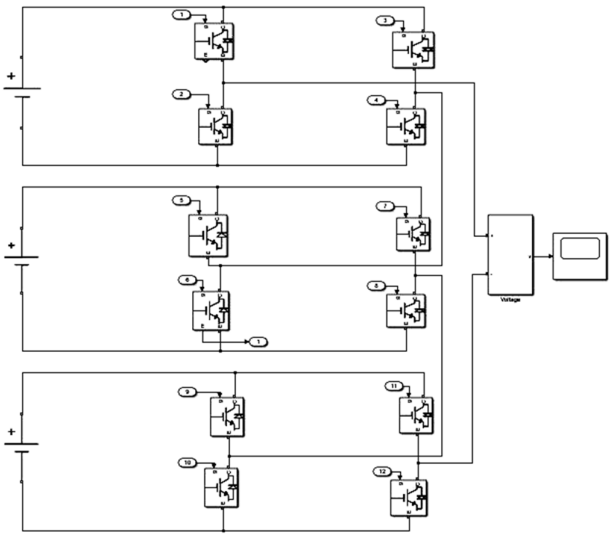

FIGURE 3. MATLAB-Simulink model of 7 levels cascaded MLI.

Further contents of the papers are organized as: section 3 explains the research methodology, section 4 explains the reliability analysis, results and discussions are presented in section 5, comparison with existing works is mentioned in section 6, and finally the conclusion is presented in the last section.

III. METHODOLOGY

In this section, the structure of the FT-CHB-MLI is discussed; then the schematics of the Cascaded 7-level H-bridge inverter are elaborated and after that, the fault analysis of a switch in case of an open circuit is done.

A. 7 LEVEL CASCADED MLI

The proposed 7-level cascaded MLI is designed using three cascaded H-bridges to achieve the desired seven-level output. Each bridge constitutes four different IGBT/MOSFET switches, and a total of three bridges are used to complete the design model. Overall, twelve IGBT/MOSFETs are used as power electronic switches to shift the converter output into seven levels. Figure 3 depicts the complete circuit of the design model which is implemented in MATLAB-Simulink. Meanwhile, three isolated DC batteries of 100V each are connected with H-bridge to get a peak output level of 300V.

In the simulation circuit, there are 12 IGBT modules with diodes in reverse of each IGBT module. The DC voltage source across each of the IGBT modules with a magnitude of 100 V. whereas, the sinusoidal voltage for the triggering of IGBT modules is 1.5sin 50t. The NOT operators are used for alternative selections of the IGBT modules during output waveform generation. This is a conventional circuit in which there is no fault and without any fault-tolerant circuit.

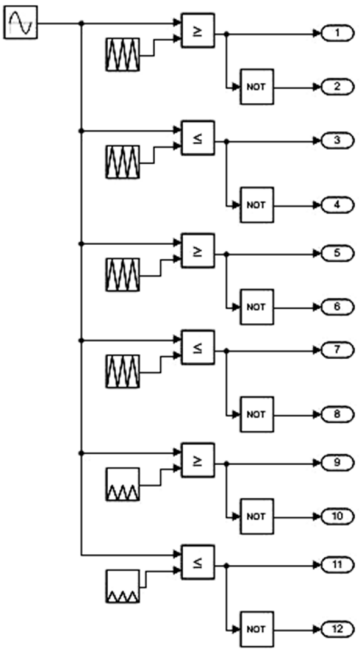

FIGURE 4. MATLAB-Simulink model of Phase disposition pulse sinusoidal width modulation.

B. PHASE DISPOSITION SINUSOIDAL PULSE WIDTH MODULATION

In paper [24], a Phase Disposition Pulse Width Modulation (PD-PWM) technique for a three-phase five-level NPC-MLI is proposed, which employs a mathematically formulated harmonic mitigation algorithm to reduce the high-frequency Weighted Total Harmonic Distortion (WTHD) content of the inverter output voltage. The practical findings of a three-phase NPC-MLI prototype are quite similar to the suggested control scheme's theoretical calculation and simulated outcomes. Furthermore, a quantitative comparison analysis confirms that the suggested PD-PWM approach has the lowest WTHD content of all the previously presented PWM schemes under consideration, confirming the proposed work's superiority. In [25], a modified rotative PD-PWM (MPD-PWM) technique was suggested to overcome the problem of uneven power distribution. The switching losses were overcome by injecting a common-mode voltage into the PWM modulator.

The phase disposition sinusoidal pulse width modulation (PDSPWM) comprises a reference sinusoidal signal of 50HZ and 1.5 magnitudes, and six rectangular carrier waves each width a magnitude of 0.5 and 1000Hz carrier frequency are in the same phase, while three carrier waves are above and three are below the zero reference line as shown in Figure 4. All the carriers are in the same phase in this method of PWM. The input sinusoidal signals and carrier waves are shown in Figure 5.

C. FAULT ANALYSIS OF AN OPEN CIRCUIT SWITCH FOR CASCADED H-BRIDGE 7-LEVEL INVERTER

Numerous plausible reasons are possible for the occurrence of faults in power devices used for switching. Their main

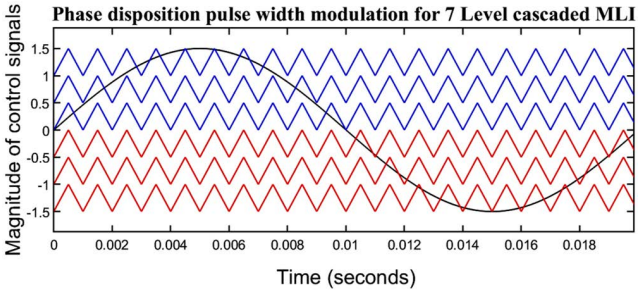

FIGURE 5. Input signals of the phase disposition pulse sinusoidal width modulation.

reason is due to switches. The main causes of switch failure are a huge and sudden drop of load or DC voltage source will be suddenly increased or decreased, due to load. On the load side, there is a possibility of a short circuit or an open circuit of a phase i.e. two phases or a phase to earth and a phase to phase fault. The causes for these failures are:

1. Semiconductor material quality issues result in the breakdown of the device.
2. The fault of a gate driving source either pulsating transformer or any other source
3. Wrong triggering of gate results in undesired results.
4. Breakdown due to heat (thermal breakdown).

The above reasons will, at last, take us to below 2 types of faults:

1. Open Circuit Fault of Switch
2. Short Circuit Fault of Switch [26]

Short Circuit faults are not much considered, so discussion and analysis of the open circuit faults are done only. Regarding the open circuit faults in a 7-level cascaded MLI, it is clear that there are 12 switches for each phase. From this one can infer that the total no. of switches for a 3-ϕ 7-level Cascaded MLI will be 36 which is quite a tedious task to determine the faulty switch location for which an algorithm was developed to find out if the faulty switch has an open circuit fault. The algorithm is shown in Figure 6. It describes that in case of fault occurrence, the procedure of its identification is divided into two sections:

1) Total Harmonics Distortion Measurement
2) Normalized voltage Factor [27]

The THD measurement will identify the phase which is faulty. In this way, our inspection is reduced to 12 switches from 36. The phase in which the switch is faulty will have a higher THD with respect to the other phases. After that, we cater to the 12 switches by the normalized voltage factor technique. In this technique, a comparison between the threshold value and the normalized factor one is done. So the faulty switch location will be found [29].

1) THD MEASUREMENT OF Vout PHASE

The THD of any Vout phase is measured using the Fast Fourier Transform (FFT). If any phase has an open circuit fault, the THD of that phase will be extremely high when compared to the others. To compare it to the Tx value,

Tmin (Minimum Threshold) is employed. For an open circuit switch fault, the Txth value is the count of total harmonic distortions [28]. This number is compared to Tx. So, once the problematic phase has been identified, we'll utilize the Vxn (normalized voltage) technique to locate the phase's bad switch.

2) NORMALIZED VOLTAGE FACTOR

Vxn normalized voltage factor is defined as the ratio of Vxav (Respective phase average voltage) to Vs (Park's Transformation output voltage). It's possible to write it as:

$$V_{Xn} = \frac{V_{Xav}}{V_s} \tag{3}$$

here

$$V_s = V_d + V_q \tag{4}$$

$$V_d = \frac{2}{3}V_a - \frac{1}{3}(V_b + V_c) \tag{5}$$

and

$$V_q = \frac{1}{\sqrt{3}}(V_b - V_c) \tag{6}$$

The odd number of switches will miss/generate positive levels of output voltage, whereas the even number of switches will miss/generate negative levels of output voltage. When a malfunction occurs, it may be easily monitored. As per the algorithm, the value of the normalized voltage factor (V_{Xn}) is almost zero in normal conditions i.e. no fault is occurring. Now, if any fault occurs, that value will shift from zero. The shifted value is relying on the switch (faulty one). If the fault is less than zero then a possibility will be on the negative side. The value V_{Xn} is then matched with the V_{uth} and V_{lth}. V_{lth} is the lower threshold voltage and the V_{uth} is the upper threshold voltage. If the value of the matching is "NO", the possible faulty switch is SX8, So the output variable i.e. dx will be 0. It will be 1 if the comparison result is "YES". In this case, SX2, SX4, SX6, SX10, and SX12 are possible locations of fault. The result would be quite an opposite i.e. the odd no. of switches will be the faulty ones if the value of deviation is <0. The value is then analyzed by V_{Xn} & V_{lth}. If the value analyzed is "YES" then the variable ux will be 1 [17]. In that case, the possibility of the faulty switches could be SX3, SX5, SX7, SX9, and SX11. If the result is a "NO", then the faulty switch will be SX1 and the value of the variable will be zero. These variables can be written mathematically as:

$$d_x = \begin{cases} 1, & \forall V_{Xn} \geq V_{uth} \\ 0, & \forall V_{Xn} \geq V_{uth} \end{cases} \tag{7}$$

$$u_x = \begin{cases} 1, & \forall V_{Xn} \geq V_{lth} \\ 0, & \forall V_{Xn} \geq V_{lth} \end{cases} \tag{8}$$

D. SIMULATION CIRCUIT

The proposed fault-tolerant control system for IGBT-based 7-level cascaded MLI has been implemented in MATLAB and Simulink environment and is shown in Figure 7.

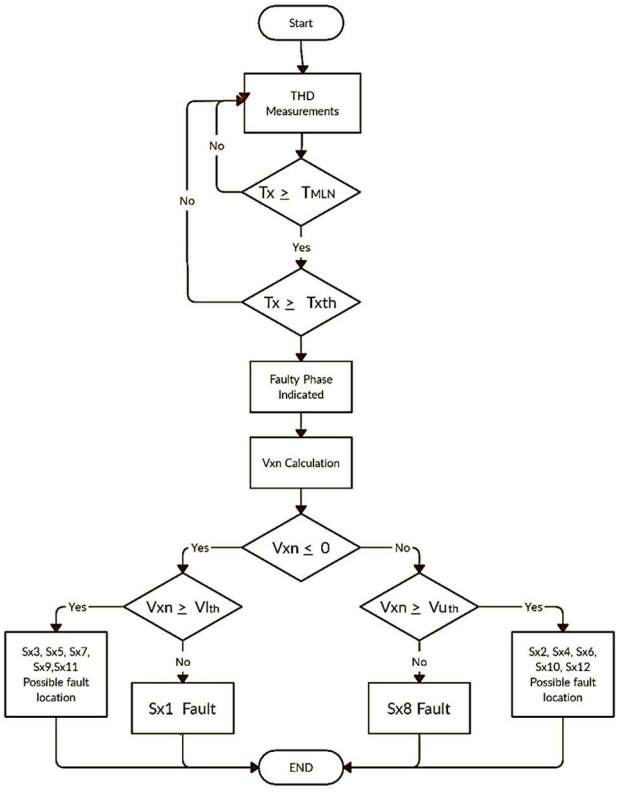

FIGURE 6. Algorithm of fault diagnosis [29].

To explain this model in a better way, it has been divided into three major parts i.e. phase disposition-based pulse width modulation system, fault detection, and isolation system, and power electronics-based model of 7 levels cascaded MLI.

The model consists of individual subunits as follows:

1. Fault Injection Unit
2. Phase Disposition Unit
3. Fault Injection Block
4. Fault Detection and Isolation Unit
5. 7-Level CHB MLI

The Fault Injection Unit (FIU) has been shown in Figure 8 in which the control of 12 IGBT switches has been shown. The switch is made by pressing the slider switch to the Fail position.

The fault control block is shown in Figure 9. The block receives the command from the FIU. For the true value of the switch, the value of 1 is passed and for a faulty switch, the ramp down signal is passed with becomes zero after a time delay of 0.2 sec.

The proposed redundant, fault-tolerant system is implemented for the operation of 7-levels cascaded MLI in Simulink, as shown in Figure 10.

The FDI unit, shown in Figure 11, is one of the main components of this research work and is an essential component of an AFTCS architecture. It consists of the control system for two different outputs i.e. one from the main IGBT and the other from the standby IGBT. During normal operation, output from the regular IGBT is provided to the power circuit.

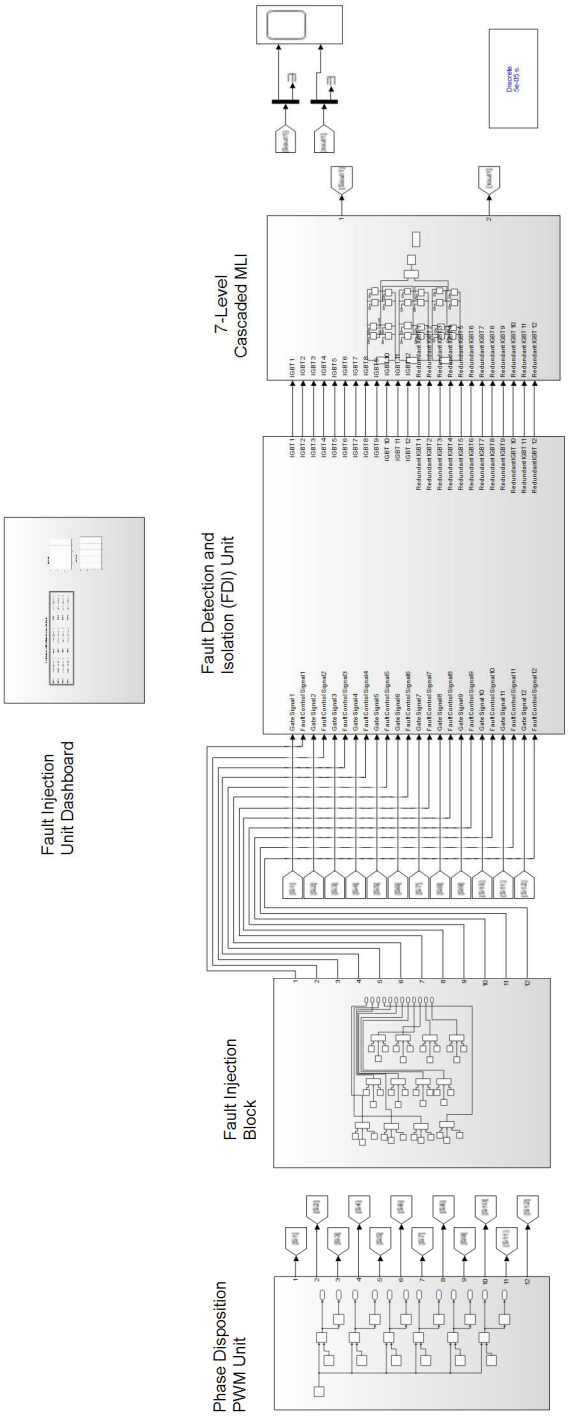

FIGURE 7. Proposed FT-CHB-MLI model.

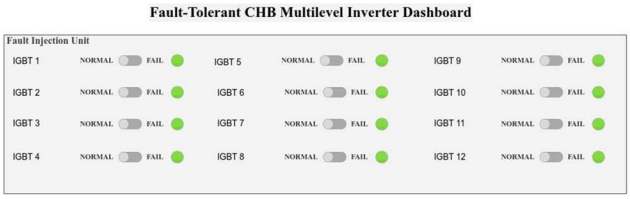

FIGURE 8. Fault injection unit (FIU).

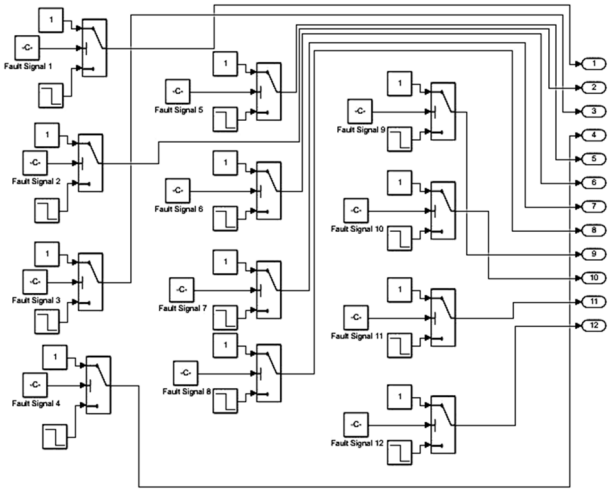

FIGURE 9. Fault-tolerant control block.

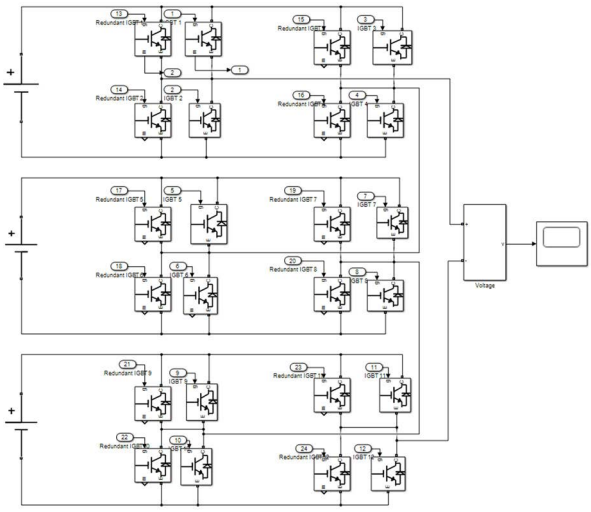

FIGURE 10. FT-CHB-MLI simulink switches model.

However, in case of fault, the faulty switch is located and isolated. The output from the standby switch is then provided to the power circuit with a slight delay incorporated as per the practical scenario. The internal blocks for the switches in the FDI unit are shown in Figure 12.

The fault detection unit of the FDI unit has two indications. The first is a constant zero signal block, which indicates that the redundant IGBT is turned off while the primary IGBT is operational. The second signal, as illustrated in Figure 13, is the healthy signal, which is utilized to turn on the primary IGBT. The fault control signal actuates the switch and isolates the faulty switch by supplying no gate signal to it while simultaneously applying the gate signal to redundant IGBTs as the fault is injected.

The work assumes that the switching activity of IGBTs takes place in zero time. It is also assumed there are no losses in the switches. The work's limitations include an increase in the total system's physical size, weight, complexity,

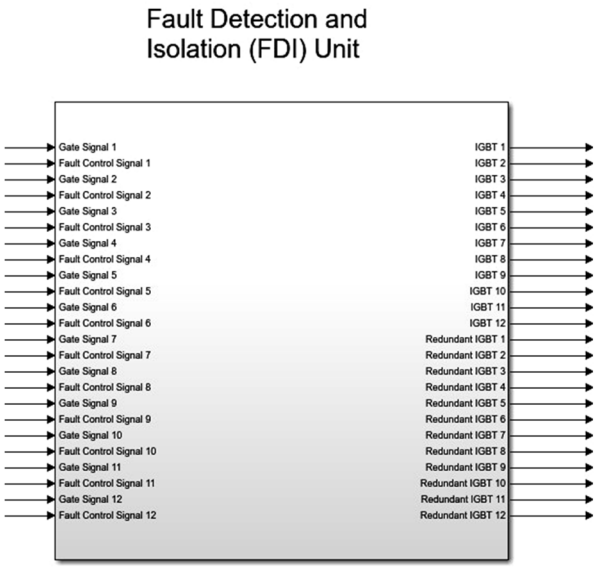

FIGURE 11. Fault detection and isolation (FDI) unit.

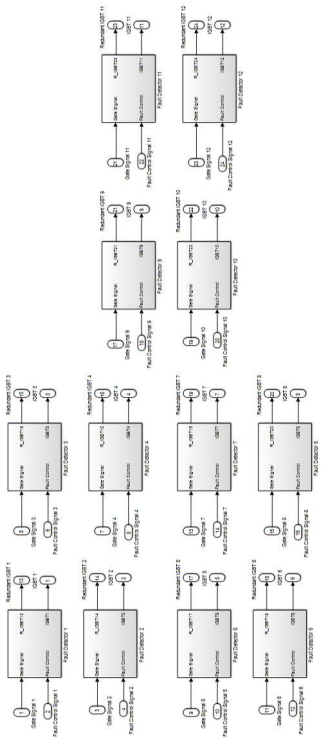

FIGURE 12. Internal blocks of FDI unit.

and expense due to hardware redundancy. If both redundant switches fail at the same time, the recommended solution will fail and the system will shut down. Furthermore, ideal switches with zero resistance in the closed state and infinite resistance in the open state are explored. These, on the other hand, have low closed resistance and a large finite resistance in the open state. The paper is very much focused on the development of AFTCS with an FDI unit for fault detection, isolation, and reconfiguration with a redundant standby

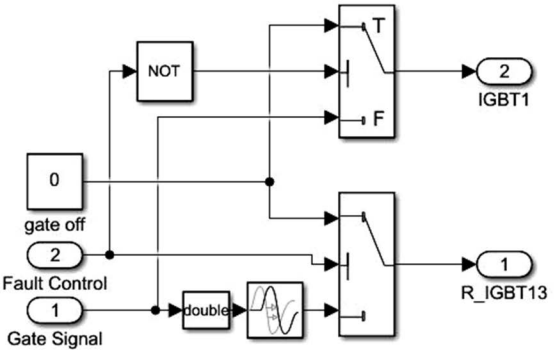

FIGURE 13. FTC switching model.

switch. Total harmonic distortion and the determination of a normalized output voltage factor are employed for fault diagnosis. The Phase Disposition Pulse Width Modulation (PD-PWM) technique was utilized for switching due to its superior performance as compared to other conventional techniques. Load variations and impact on the performance of the proposed FTC algorithm were not studied and mentioned in the limitations of the paper.

IV. RELIABILITY ANALYSIS

The suggested FT-CHB- MLI's reliability has been assessed using Markov chains in this section. The Mean Time to Failure is one of the most important quantitative indicators of a system's reliability. The mean time to failure (MTTF) of an item is displayed. It is the average amount of time that an item is predicted to last in service. The failed item has an indefinite repair time or simply cannot be fixed, according to the MTTF modeling assumption [28]. The following formula is used to calculate MTTF:

$$MTTF = \int_0^\infty R(t)\,dt \tag{9}$$

MTTF can also be calculated by taking the reciprocal of failure rate (λ) as follows:

$$MTTF = \frac{1}{\lambda} \tag{10}$$

For the whole MLI assembly, we get

$$\lambda_1 = (2N-1)\,\lambda_0 \tag{11}$$

where λ_0 is the failure rate of a single IGBT switch. By differentiation, we get

$$\frac{dP_1}{dt} = -2\lambda_1 P_1(t) \tag{12}$$

Hence,

$$R(t) = P_1(t) = e^{-2(2N-1)\lambda_0 t} \tag{13}$$

where N represents the number of switch modules in the MLI. Without fault tolerance, we get

$$MTTF_{without\ FTC} = \frac{1}{2\lambda_0}\left(\frac{1}{2N-1}\right) \tag{14}$$

$$\lambda_1 = \left(\frac{2N-1}{2} + 1\right)\lambda_0 \tag{15}$$

The failure rate of the two modules would be as follows:

$$\lambda_2 = \left(\frac{2N-1}{2}\right)\lambda_0 \tag{16}$$

From Markov chains, we get

$$\frac{dP_1}{dt} = -\lambda_1 P_1(t) \tag{17}$$

$$P_1(t) = e^{-(\frac{2N-1}{2}+1)\lambda_0 t} \tag{18}$$

$$\frac{dP_1}{dt} = \lambda_1 P_1(t) - \lambda_2 P_2(t) \tag{19}$$

$$P_2(t) = \left(\frac{2N-1}{2}\right)(e^{-\left(\frac{2N-1}{2}\right)\lambda_0 t} - e^{-\left(\frac{2N-1}{2}+1\right)\lambda_0 t} \tag{20}$$

The total reliability would be as follows:

$$\begin{aligned} R(t) &= P_1(t) + P_2(t) \\ &= \left((\frac{1-2N}{2})e^{-\left(\frac{2N-1}{2}+1\right)\lambda_0 t}\right) \\ &\quad + \left(\frac{2N-1}{2}\right)(e^{-\left(\frac{2N-1}{2}\right)\lambda_0 t}) \end{aligned} \tag{21}$$

$$MTTF_{withFTC1} = \frac{1}{\lambda_0}(\frac{1-N}{N+1}) \tag{22}$$

$$\lambda_2 = (2N-3)\lambda_0 \tag{23}$$

$$\frac{dP_1}{dt} = -(\lambda_1+\lambda_2)P_2(t) - \lambda_1 P_1(t) \tag{24}$$

$$P_2(t) = \left(\frac{2N-3}{2}\right)(e^{-(\lambda_1+\lambda_2)t} - e^{-2\lambda_1 t}) \tag{25}$$

$$\frac{dP_4}{dt} = -(2\lambda_2)P_4(t) + \lambda_1 P_2(t) + \lambda_1 P_3(t) \tag{26}$$

$$\begin{aligned} P_4(t) &= \frac{(2N-3)^2}{4}\left(e^{-2\lambda_1 t} + e^{-2\lambda_2 t}\right) \\ &\quad - \frac{(2N-3)^2}{2}e^{-(\lambda_1+\lambda_2)t} \end{aligned} \tag{27}$$

$$R(t) = P_1(t) + P_2(t) + P_3(t) + P_4(t) \tag{28}$$

$$\begin{aligned} R(t) &= \left((2N-2) + \frac{(N-3)^2}{4}\right)e^{-2(2N-1)\lambda_0 t} \\ &\quad + \left((2N-3) + \frac{(2N-3)^2}{4}\right)e^{-2(2N-2)\lambda_0 t} \\ &\quad + \left(\frac{(2N-3)^2}{4}\right)e^{-2(2N-3)\lambda_0 t} \end{aligned} \tag{29}$$

$$\begin{aligned} MTTF_{with\ FTC} &= \frac{1}{2\lambda_0}(\frac{\left((2N-2) + \frac{(2N-3)^2}{4}\right)}{(2N-1)} \\ &\quad + \frac{\left((2N-3) + \frac{(2N-3)^2}{4}\right)}{(2N-2)} + \frac{(\frac{(2N-3)^2}{4})}{(2N-3)}) \end{aligned} \tag{30}$$

The equation demonstrates that the MTTF has significantly increased with the proposed FT-CHB-MLI architecture.

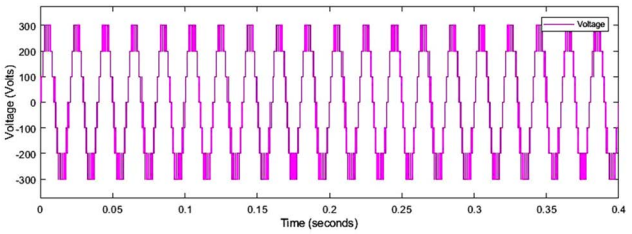

FIGURE 14. The output waveform of the 7-level cascaded inverter without any fault.

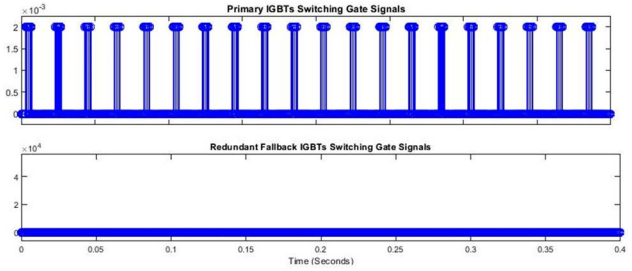

FIGURE 15. Switching pattern without fault.

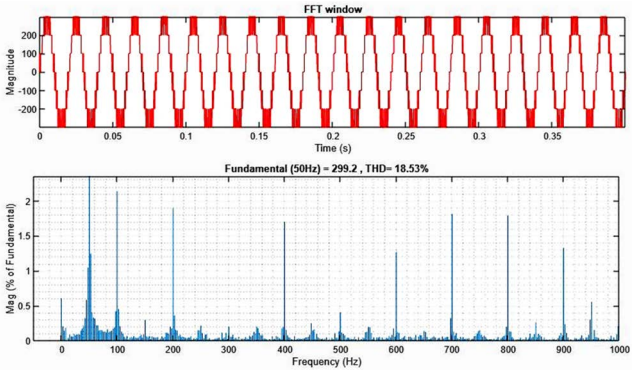

FIGURE 16. THD without fault.

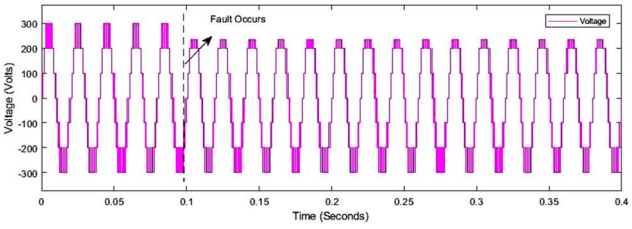

FIGURE 17. Output waveform with fault.

V. RESULTS AND DISCUSSIONS

The output voltages of the proposed 7-level cascaded MLI are shown in Figure 14. These output voltages have a magnitude of 300V (peak). As in this situation, there is no fault applied at any switch of the MLI, therefor output voltages are equal throughout the simulations.

The switching signals to the primary IGBTs during normal operation are shown in Figure 15. The standby redundant IGBTs remain in the off condition with no switching signal.

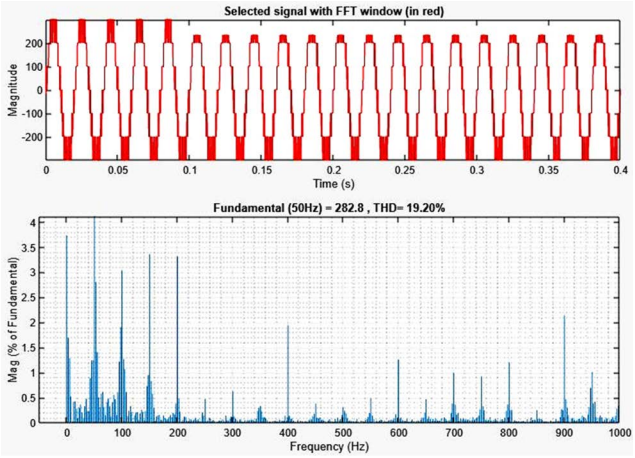

FIGURE 18. THD with fault.

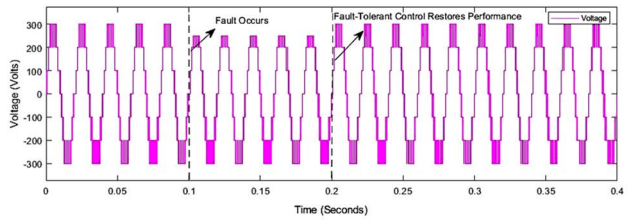

FIGURE 19. Output waveform with FTC.

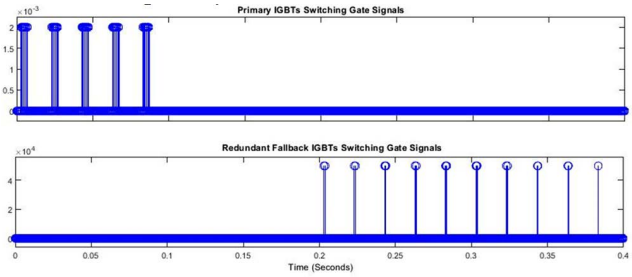

FIGURE 20. Switching pattern with FTC.

The THD has been measured using the FFT tool of Simulink. Figure 16 shows a total THD of 18.53% for the normal operation of this CHD MLI.

Now the fault is injected by the FIU at 0.1 seconds and the resulting output waveform is shown in Figure 17.

The positive peak voltage has reduced to around 200 V and total THD has also increased to 19.2% as shown in Figure 18.

Now the system has been simulated with FTC CHB MLI configuration and the resulting waveform is shown in Figure 19. The results show that the output is affected at 0.1 seconds at the time of fault injection but returns to its normal operation due to the switch over of the faulty switch to the healthy standby IGBT switch.

The switching states of both primary and standby IGBTs after the occurrence of fault are shown in Figure 20 which shows the operation of the redundant switch due to the failure of the primary switch.

The THD of the output waveform of FT CHB MLI is shown in Figure 21 which shows the improvement from

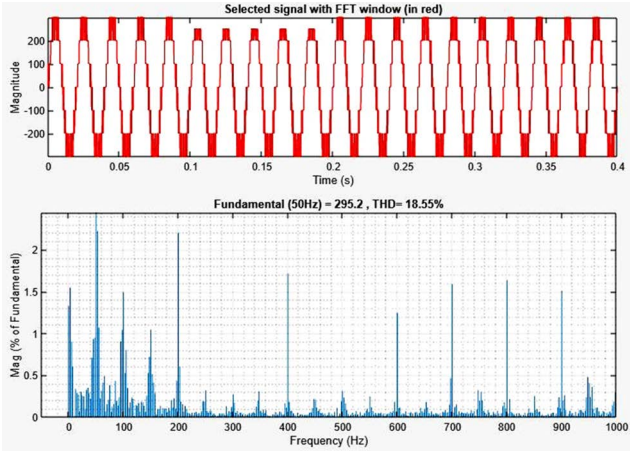

FIGURE 21. THD with FTC.

TABLE 2. Comparison of the previous and proposed model.

Component	Reference [16]	Reference [29]	Proposed Work
Power Switches	8	8	24
THD	48.3 %	20.83%	18%
Reliability	Moderate	High	High
Complexity	Simple	High	Moderate
Switching Technique	PWM	LSPWM	PD-PWM

19.2% to 18.55% by the proposed control system. Hence, the objective of reliability enhancement with improved power quality has been successfully achieved.

VI. COMPARISON WITH EXISTING WORKS

In this section, a comparison of the proposed FT-CHM-MLI has been performed to demonstrate its superior performance.

In [16], a fault-tolerant H-bridge system is proposed for DC motor speed control with the PWM technique only resulting in a very large harmonics content of about 48.3% in the output waveform which makes the proposed solution not feasible from the power quality point of review through its highly reliable. The solution proposed in [29], FT-CHB is proposed but it is only for five levels that also results in a high THD of 20.83% which is not up to the mark. In this proposed work, the THD has been reduced to almost 18% with a significant increase in reliability with advanced fault-tolerant architecture consisting of an FDI unit, as shown in Table 2.

VII. CONCLUSION

In this paper, a novel 7-level Fault-Tolerant Cascaded H-Bridge Multilevel Inverter (FT-CHB-MLI) was proposed that offers high reliability with improved power quality. A dedicated Fault Detection and isolation (FDI) unit was built to diagnose the faulty switch and replace it with a standby redundant switch. Total harmonic distortion and the determination of a normalized output voltage factor were employed for fault diagnosis. The Phase Disposition Pulse

Width Modulation (PD-PWM) technique was utilized for switching due to its superior performance as compared to other conventional techniques. The proposed system was experimentally tested on the MATLAB / Simulink environment to verify its performance. The simulation results demonstrated that the THD has been reduced to almost 18% with a significant increase in reliability with advanced fault-tolerant architecture consisting of FDI units. The reliability analysis was carried out using Markov chains that also showed its increased reliability. A comparison of the proposed work with literature also depicted its superior performance in achieving its superior power quality and increased reliability.

A more sophisticated FTC technique using artificial intelligence in the future could more precisely pinpoint the Fault location with a better understanding with hardware experimental verification. Another direction is to study the effect of load variations and variations in the modulation index on the performance proposed AFTCS.

REFERENCES

[1] S. Daher, J. Schmid, and F. L. M. Antunes, "Multilevel inverter topologies for stand-alone PV systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2703–2712, Jul. 2008, doi: 10.1109/TIE.2008.922601.

[2] A. Dekka, O. Beik, and M. Narimani, "Modulation and voltage balancing of a five-level series-connected multilevel inverter with reduced isolated direct current sources," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8219–8230, Oct. 2020, doi: 10.1109/TIE.2019.2949537.

[3] S. A. González, M. I. Valla, and C. F. Christiansen, "Five-level cascade asymmetric multilevel converter," *IET Power Electron.*, vol. 3, no. 1, p. 120, 2010, doi: 10.1049/iet-pel.2008.0318.

[4] S. S. Lee, "Single-stage switched-capacitor module (S3CM) topology for cascaded multilevel inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8204–8207, Oct. 2018, doi: 10.1109/TPEL.2018.2805685.

[5] G. Konstantinou, S. R. Pulikanti, M. Ciobotaru, V. G. Agelidis, and K. Muttaqi, "The seven-level flying capacitor based ANPC converter for grid intergration of utility-scale PV systems," in *Proc. 3rd IEEE Int. Symp. Power Electron. Distrib. Gener. Syst. (PEDG)*, Jun. 2012, pp. 592–597.

[6] P. N. V. S. Ayyappa, C. Srinivas, and T. R. S. Singh, "A novel way to deal with harmonic elimination in multi level CHB inverter using without filtering technique," in *Proc. Int. Conf. Electron., Commun. Aerosp. Technol. (ICECA)*, Apr. 2017, pp. 62–67.

[7] A. R. Abbaspour, "Active fault-tolerant control design for nonlinear systems," M.S. thesis, FIU Electron., 2018, vol. 3917. [Online]. Available: https://digitalcommons.fiu.edu/etd/3917

[8] Z. Ji, J. Zhao, Y. Sun, X. Yao, and Z. Zhu, "Fault-tolerant control of cascaded H-bridge converters using double zero-sequence voltage injection and DC voltage optimization," *J. Power Electron.*, vol. 14, no. 5, pp. 946–956, Sep. 2014.

[9] A. A. Amin and K. M. Hasan, "A review of fault tolerant control systems: Advancements and applications," *Meas., J. Int. Meas. Confederation*, vol. 143, pp. 58–68, Sep. 2019, doi: 10.1016/j.measurement.2019.04.083.

[10] R. F. Stengel, "Intelligent failure-tolerant control," *IEEE Control Syst. Mag.*, vol. 11, no. 4, pp. 14–23, Jun. 1991.

[11] A. A. Amin and K. Mahmood-Ul-Hasan, "Advanced fault tolerant air-fuel ratio control of internal combustion gas engine for sensor and actuator faults," *IEEE Access*, vol. 7, pp. 17634–17643, 2019.

[12] M. Sandhu and T. Thakur, "Modified cascaded H-bridge multilevel inverter for hybrid renewable energy applications," *IETE J. Res.*, vol. 1, pp. 1–13, Jul. 2020.

[13] J.-H. Lee and K.-B. Lee, "A fault detection method and a tolerance control in a single-phase cascaded H-bridge multilevel inverter," *IFAC-PapersOnLine*, vol. 50, no. 1, pp. 7819–7823, Jul. 2017.

[14] Z. Liu, Y. Lu, J. Kong, J. Gong, and S. Wang, "Multimodal fault-tolerant control for single-phase cascaded off-grid PV-storage system with PV failure using hybrid modulation," *Microelectron. Rel.*, vol. 114, Nov. 2020, Art. no. 113772.

[15] S. Khomfoi and L. M. Tolbert, "Fault detection and reconfiguration technique for cascaded H-bridge 11-level inverter drives operating under faulty condition," in *Proc. 7th Int. Conf. Power Electron. Drive Syst.*, Nov. 2007, pp. 1035–1042.

[16] S. Ahmed, A. A. Amin, Z. Wajid, and F. Ahmad, "Reliable speed control of a permanent magnet DC motor using fault-tolerant H-bridge," *Adv. Mech. Eng.*, vol. 12, no. 10, 2020, Art. no. 1687814020970311.

[17] A. A. Amin and K. Mahmood-ul-Hasan, "Robust active fault-tolerant control for internal combustion gas engine for air–fuel ratio control with statistical regression-based observer model," *Meas. Control*, vol. 52, nos. 9–10, pp. 1179–1194, Nov. 2019.

[18] K.-H. Chao and C.-H. Ke, "Fault diagnosis and tolerant control of three-level neutral-point clamped inverters in motor drives," *Energies*, vol. 13, no. 23, p. 6302, Nov. 2020.

[19] U. Riaz, M. Tayyeb, and A. A. Amin, "A review of sliding mode control with the perspective of utilization in fault tolerant control," *Recent Adv. Electr. Electron. Eng., Formerly Recent Patents Electr. Electron. Eng.*, vol. 14, no. 3, pp. 312–324, Apr. 2021.

[20] P. Lezana, R. Aguilera, and J. Rodríguez, "Fault detection on multicell converter based on output voltage frequency analysis," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2275–2283, Jun. 2009.

[21] J. Druant, T. Vyncke, F. De Belie, P. Sergeant, and J. Melkebeek, "Adding inverter fault detection to model-based predictive control for flying-capacitor inverters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 4, pp. 2054–2063, Apr. 2015.

[22] H.-W. Sim, J.-S. Lee, and K.-B. Lee, "Detecting open-switch faults: Using asymmetric zero-voltage switching states," *IEEE Ind. Appl. Mag.*, vol. 22, no. 2, pp. 27–37, Mar. 2016.

[23] A. A. Amin and K. Mahmood-ul-Hasan, "Hybrid fault tolerant control for air–fuel ratio control of internal combustion gasoline engine using Kalman filters with advanced redundancy," *Meas. Control*, vol. 52, nos. 5–6, pp. 473–492, Jun. 2019, doi: 10.1177/0020294019842593.

[24] R. Sarker, "Phase disposition PWM (PD-PWM) technique to minimize WTHD from a three-phase NPC multilevel voltage source inverter," in *Proc. IEEE 1st Int. Conf. Converg. Eng. (ICCE)*, Sep. 2020, pp. 220–224, doi: 10.1109/ICCE50343.2020.9290697.

[25] D. Ronanki and S. S. Williamson, "Modified phase-disposition PWM technique for modular multilevel converters," in *Proc. IEEE Transp. Electrific. Conf. Expo (ITEC)*, Jun. 2018, pp. 26–31, doi: 10.1109/ITEC.2018.8450084.

[26] Y. Zang, X. Wang, B. Xu, and J. Liu, "Control method for cascaded H-bridge multilevel inverter failures," in *Proc. 6th World Congr. Intell. Control Autom.*, vol. 2, 2006, pp. 8462–8466.

[27] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[28] M. Abdelsalam, H. Diab, S. Tennakoon, and A. Griffiths, "Reliability enhancement of modular multilevel converter by applying fault tolerant control," in *Proc. 51st Int. Univ. Power Eng. Conf. (UPEC)*, Sep. 2016, pp. 1–5, doi: 10.1109/UPEC.2016.8114008.

[29] P. Mehta, S. Sahoo, and M. Kumar, "A fault-diagnosis and tolerant control technique for five-level cascaded H-bridge inverters," *IET Circuits, Devices Syst.*, vol. 15, no. 4, pp. 366–376, 2021.

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