An Improved Control System for Modular Multilevel Converters with New Modulation Strategy and Voltage Balancing Control

Shengfang Fan, *Student Member, IEEE*, Kai Zhang, Jian Xiong, and Yaosuo Xue, *Senior Member, IEEE*

***Abstract*—Modular multilevel converter (MMC) has become one of the most promising converter topologies for future high-power applications. A challenging issue of the MMC is the voltage balancing among arm capacitors. A good overall control system is also vital for the MMC, which should be based on sound mathematical model, readily adaptable for different applications, and capable of high performance. This paper presents a general control structure for MMC inverters, which is suitable for both voltage-based and energy-based control methods, and includes voltage balancing between the upper and lower arms. A new method for voltage balancing among arm capacitors, which is based on an improved pulse-width modulation, is also presented. The proposed method avoids some major disadvantages found in present voltage balancing methods, such as dependence on computation-intensive voltage sorting algorithms, extra switching actions, interference with output voltage, etc. Furthermore, all switching actions are evenly distributed among power devices. The proposed control system as a whole can serve as a promising solution for practical applications, especially when the number of submodules is fairly high. Simulation and experimental results verify the effectiveness of the proposed methods.**

***Index Terms*—Control structure, modulation, modular multilevel converter (MMC), voltage balancing control.**

I. Introduction

RECENTLY, multilevel converters have attracted growing attentions and found themselves in increasing market of high power and high/medium voltage applications [1], [2], such as high-voltage dc transmission (HVDC), flexible ac transmission systems (FACTS), industrial motor drives, utility-scale renewable energy systems, and so on. Among various multilevel converters, the diode-clamped or neutral-point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) are the most studied topologies [3]–[7]. However, for the applications requiring more than four or five levels, the NPC and FC topologies become less attractive due to significantly increased number of clamping diodes or FCs, higher power losses, and difficulty to balance the capacitor voltages [3]–[6]. The CHB topology then seems more suitable due to its modular structure. However, it requires a large number of isolated dc sources, which are often provided by a bulky, multiwinding transformer together with a series of rectifiers [7].

To eliminate the need for separate dc sources, a modular multilevel converter (MMC or M2C) topology composed of half-bridge or chopper submodules (SM) was proposed [8]. It has become more and more attractive due to the modular structure, common dc-bus, distributed dc capacitors, easy grid connection, simple realization of redundancy, etc. [8]–[11].

As so far, voltage balancing of the floating SM capacitors remains one of the major challenges of the MMC, and has called upon many researches in the last few years [13]–[23]. The present voltage balancing methods can be roughly categorized into two groups: distributed methods and centralized methods. The distributed methods keep the voltage of each capacitor close to its reference value through closed-loop control, and usually with carrier phase-shifted pulse-width modulation (CPSPWM) [13]–[15]. The balancing control is carried out with a modification of the modulating signal for the PWM process. It can achieve good voltage balancing when the switching frequency of each SM is high enough. However, changing the modulating signals of the SMs may affect the power quality at ac side [20]. Furthermore, the hardware and software cost of required SM-level controllers and PWM comparators becomes enormous when the number of SMs gets high [16].

Centralized methods achieve voltage balancing at the PWM stage. They select certain SMs for certain switching states depending on capacitor voltages and arm current polarities [8], [16]–[20], therefore are also called module selection methods. These methods are usually (but not necessarily) used with phase disposition PWM (PDPWM). A typical balancing process is as follows. During each PWM period, the SM capacitor voltages within one arm are measured and sorted, and the number of SMs to be switched on is determined. If the arm current is positive (corresponding to charging of the capacitors) or zero, the SMs with the lowest capacitor voltages will be switched ON, the SM with next-lowest capacitor voltage will be PWM switched, and the rest will be switched OFF. The opposite thing happens if the arm current is negative. This strategy yields good voltage balancing, but the voltage sorting algorithm have to be executed at the equivalent switching frequency of one arm, posing a heavy computational burden when the number of SMs is high. Another problem of this strategy is the extra switching actions, which

Manuscript received August 30, 2013; revised December 17, 2013; accepted January 23, 2014. Date of publication February 6, 2014; date of current version August 26, 2014. Recommended for publication by Associate Editor Z. Xu.

S. Fan, K. Zhang, and J. Xiong are with the State Key Laboratory of Advanced Electromagnetic Engineering and Technology, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: shengfangfan@hust.edu.cn; kaizhang@hust.edu.cn; xjhustwh@sina.com).

Y. Xue is with the Corporate Technology, Siemens Corporation, Princeton, NJ 08540 USA (e-mail: yaosuo.xue@siemens.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2014.2304969

are generated in the aforementioned process solely for the sake of voltage balancing and unnecessary for the synthesis of output voltage [19].

An improved centralized method is proposed in [19], where if extra SMs need to be switched ON, only the SMs that are currently OFF can be select (and vice versa). It reduces the average device switching frequency by avoiding extra switching actions. However, the voltage balancing accuracy is compromised. Besides, the high-frequency voltage sorting is still required. In this regard, Mei *et al.* in [20] proposed a new method which only looks up and adjusts the capacitors with the highest and lowest voltages. Nevertheless, the problem of extra switching actions still exists, albeit alleviated to some extent.

Ilves *et al.* proposed a centralized method [21] with selective harmonic elimination PWM and open-loop control. Voltage balancing can be achieved after a large number of fundamental periods. However, it brings low-frequency ripples into the capacitor voltages, and the ripple frequency is inversely proportional to the number of SMs in one arm. Consequently, larger capacitors are required to suppress the ripple voltage. Furthermore, the open-loop control cannot guarantee the voltage balancing under all operating conditions [22].

Deng *et al.* [23] proposed another centralized method with CPSPWM. It does not need to measure the arm currents, therefore the cost is reduced. However, high-frequency voltage sorting still remains. Moreover, this method is heavily dependent on high switching frequencies, which may not be possible when the number of SMs is large.

This paper proposes a new centralized capacitor voltage balancing method along with an improved modulation method. This method as a whole has the following features: 1) In each arm of the MMC, only one voltage reference and one carrier are needed, which greatly reduces hardware requirement compared with CPSPWM and conventional PDPWM; 2) the SMs in one arm switch ON and OFF alternately, yielding an even distribution of switching frequency among the power devices, and, therefore, a good inherent voltage balancing capability; 3) accurate voltage balancing is achieved in a closed-loop manner; 4) unnecessary switching actions and high-frequency voltage sorting problem are both avoided.

Modeling and control of the overall MMC system are also investigated in this paper. Some typical control methods have already been proposed in the literatures, such as average control [13], arm-balancing control [14], and circulating current control [19]. The energy-based modeling and a control structure incorporating total energy control and energy balancing control were proposed in [24], [25]. Current control with two rotating frames (one at grid frequency and the other at twice grid frequency) is used for HVDC applications in [26]. This paper presents a general control structure in which both voltage-based and energy-based control methods are applicable. The control structure also has good expandability, which means control of ac and dc voltage/current for four-quadrant operation can be readily embedded. Based on total energy control and energy balancing control proposed in [24]–[26], this paper investigates the mathematical model in greater detail and proposes a more practical solution. It achieves energy/voltage balancing between the upper and lower arms with a differential energy controller and a circulating current controller.

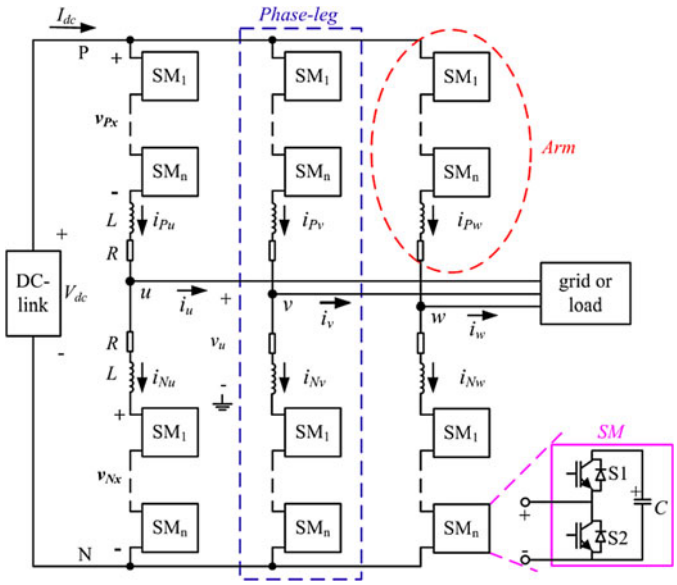


Fig. 1. Topology of modular multilevel converter.

The rest of the paper is organized as follows. Section II presents the mathematical model and control structure of the overall MMC system. Section III presents the improved modulation strategy. The new capacitor voltage balancing control based on this modulation is explained in Section IV. Simulation and experimental results are presented in Section V and VI, respectively. Section VII concludes the paper.

II. Modeling and Control Structure

A. Converter Topology

Fig. 1 shows the topology of a typical three-phase MMC. Each phase leg of the MMC consists of two arms. Each arm has N identical SMs and one smoothing inductor. Each SM has two power semiconductor switches (S1 and S2) representing two IGBTs (or other types) with freewheeling diodes and one capacitor (C). Three valid states exist for the SMs, namely ON, OFF, and standby states. When S1 is ON and S2 is OFF, the SM is in ON state and the capacitor can be charged or discharged depending on the current direction. When the capacitor is bypassed by S2, the SM is in OFF state. The standby state occurs when the SM is uncontrolled (with S1 and S2 both OFF) and the capacitor is precharged. During the two controlled states, the terminal voltage of an SM can be either zero or the capacitor voltage. In other words, the SM can provide two different voltage levels.

B. Modeling and Control Structure

The SMs in each arm can be regarded as controlled voltage sources, and they are connected in series to form a controlled voltage source with higher voltage v_{Px} and v_{Nx} $(x = u \sim w)$. In Fig. 1, $V_{\rm dc}$ and $I_{\rm dc}$ are dc-link voltage and current. i_{Px} and i_{Nx} are currents of the upper and lower arms. v_x is ac-output

voltage of phase x (with respect to the midpoint of the dc-link). v_{CPxj} and v_{CNxj} $(j = 1 \text{ to } N)$ are individual capacitor voltages in the upper and lower arms.

The basic operation principle is to control the upper-arm and lower-arm voltages to be sinusoids with dc offsets up to half dc-link voltage, but with opposite phases. By this way, the ac side phase voltage can be controlled as a sinusoid with a magnitude up to half dc-link voltage.

1) Voltage /Current Control at AC Side: According to Kirchhoff's voltage law

$$\begin{cases} \frac{1}{2}V_{\rm dc} = v_{Px} + L\frac{di_{Px}}{dt} + Ri_{Px} + v_x \\ \frac{1}{2}V_{\rm dc} = v_{Nx} + L\frac{di_{Nx}}{dt} + Ri_{Nx} - v_x \end{cases} \tag{1}$$

According to Kirchhoff's current law (KCL), ac current i_x can be expressed as

$$i_x = i_{Px} - i_{Nx}. \tag{2}$$

Define a control variable v_{1x} as

$$v_{1x} = \frac{1}{2}\left(v_{Px} - v_{Nx}\right). \tag{3}$$

Substituting (2) and (3) into (1) yields

$$\frac{1}{2}L\frac{di_x}{dt} + \frac{1}{2}Ri_x = -v_x - v_{1x}. \tag{4}$$

For grid-connected applications, the ac current (i_x) is usually controlled in a closed-loop. With this structure, all the current control methods in conventional two-level inverters can be applied. If the MMC operates as an inverter without current control, the ac voltage (v_x) is determined by v_{1x}, since the low-frequency voltage drops across the inductors are usually very small compared with v_x.

2) Voltage/Current Control at DC Side: Define a control variable v_{2x} as

$$v_{2x} = \frac{1}{2}\left(i_{Px} + i_{Nx}\right). \tag{5}$$

and circulating current i_{Zx} flowing through both the upper and low arms as

$$i_{Zx} = \frac{1}{2}\left(i_{Px} + i_{Nx}\right). \tag{6}$$

Substituting (5) and (6) into (1) yields

$$L\frac{di_{Zx}}{dt} + Ri_{Zx} = \frac{1}{2}V_{\rm dc} - v_{2x} \tag{7}$$

According to KCL

$$I_d = \sum i_{Px} = \sum i_{Nx} = \frac{1}{2}\sum(i_{Px} + i_{Nx}) = \sum i_{Zx}. \tag{8}$$

Equations (7) and (8) show that if dc-link voltage is constant, the circulating current i_{Zx} is controlled by v_{2x} and the dc component of i_{Zx} determines the average power at dc side. The circulating current also relates to the power loss and should be properly controlled.

3) Total Energy Control in Each Phase-Leg: To maintain a constant average capacitor voltage during each fundamental period, the voltages or energies stored in the capacitors of each arm should be controlled properly. The internal energies of the arms shown below are chosen as dynamic control variables

$$W_{CPx} = \sum_{j=1}^{N}\left(\frac{1}{2}Cv_{CPxj}^2\right) = \frac{1}{2}C\sum_{j=1}^{N}v_{CPxj}^2 \tag{9}$$

$$W_{CNx} = \sum_{j=1}^{N}\left(\frac{1}{2}Cv_{CNxj}^2\right) = \frac{1}{2}C\sum_{j=1}^{N}v_{CNxj}^2. \tag{10}$$

The total energy (W_{Cx}^{Σ}) and the differential energy (W_{Cx}^{Δ}) in each phase-leg are

$$W_{Cx}^{\Sigma} = W_{CPx} + W_{CNx} \tag{11}$$

$$W_{Cx}^{\Delta} = W_{CPx} - W_{CNx}. \tag{12}$$

Ignoring power losses, the power relationships are

$$\frac{dW_{CPx}}{dt} = \left(\frac{1}{2}V_{\rm dc} - v_x - L\frac{di_{Px}}{dt} - Ri_{Px}\right)i_{Px} \tag{13}$$

$$\frac{dW_{CNx}}{dt} = \left(\frac{1}{2}V_{\rm dc} + v_x - L\frac{di_{Nx}}{dt} - Ri_{Nx}\right)i_{Nx}. \tag{14}$$

Since the inductors in each phase-leg are used to filter the switching frequency harmonics, the ac-side voltage and current can be assumed to be sinusoidal

$$\begin{cases} v_x = V_x\sin(\omega t) \\ i_x = I_x\sin(\omega t - \emptyset) \end{cases} \tag{15}$$

Substituting (13)–(15) into (11) yields

$$\begin{aligned} \frac{dW_{Cx}^{\Sigma}}{dt} &= V_{\rm dc}i_{Zx} - v_x i_x - \left(L\frac{di_{Px}}{dt} + Ri_{Px}\right)i_{Px} - \left(L\frac{di_N}{dt} + Ri_{Nx}\right)i_{Nx} \\ &= V_{\rm dc}i_{Zx} - v_x i_x - 2Ri_{Zx}^2 - Ri_x^2 - 2L\frac{di_{Zx}}{dt}i_{Zx} - \frac{1}{2}L\frac{di_x}{dt}i_x \\ &= \left[V_{\rm dc}i_{Zx} - \frac{1}{2}V_x I_x\cos\emptyset - 2Ri_{Zx}^2 - R\left(\frac{i_x}{2}\right)^2\right] \\ &\quad + \left[\frac{1}{2}V_x I_x\cos(2\omega t - \emptyset) + R\left(\frac{i_x}{2}\right)^2\cos(2\omega - 2\emptyset)\right. \\ &\quad \left. - \frac{1}{2}\omega LI_x^2\sin(2\omega t - 2\emptyset) - 2L\frac{di_{Zx}}{dt}i_{Zx}\right]. \end{aligned} \tag{16}$$

It is known that i_{Zx} contains dc component (I_{Zx}) and low-frequency components (mainly second-order component, i_{2Zx}). Neglecting power loss across the equivalent resistor (R), (16) can be simplified into

$$\frac{dW_{Cx}^{\Sigma}}{dt} \approx p_{0Cx}^{\Sigma} + p_{2Cx}^{\Sigma} + p_{4Cx}^{\Sigma} \tag{17}$$

$$p_{0Cx}^{\Sigma} = V_{\rm dc}I_{Zx} - \frac{1}{2}V_x I_x\cos\emptyset \tag{18}$$

$$\begin{aligned} p_{2Cx}^{\Sigma} &= V_{\rm dc}i_{2Zx} + \frac{1}{2}V_x I_x\cos(2\omega t - \emptyset) - \frac{1}{2}\omega LI_x I_{1Zx} \\ &\quad \times\sin(2\omega t - 2\emptyset) - 2LI_{Zx}\frac{di_{2Zx}}{dt} \end{aligned} \tag{19}$$

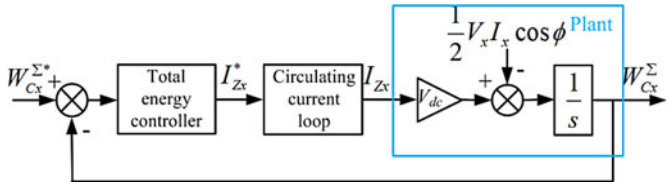


Fig. 2. Total energy control.

$$p_{4Cx}^{\Sigma} = -2L\frac{di_{2Zx}}{dt}i_{2Zx}. \tag{20}$$

As shown in (17), the power flowing from/into the capacitors in each phase-leg consists of dc component (p_{0Cx}^{Σ}) and low-frequency ripples (p_{2Cx}^{Σ} and p_{4Cx}^{Σ}). Ignoring the ripples, the total energy (W_{CPx}^{Σ}) stored in the capacitors is controlled by the dc component (p_{0Cx}^{Σ}). As a result, if the MMC works as an inverter, the dc-link voltage and the active power at ac side will be constant in steady state, then the output of W_{Cx}^{Σ} control (total energy control or average voltage control) can be a compensation added to the current I_{Zx}. Similarly, if the MMC works as a rectifier, the amplitude of ac voltage and the power at dc side are constant in steady state. In this case, the output of W_{Cx}^{Σ} control can be regarded as a compensation added to the active current $(I_x \cos \emptyset)$ at ac side. The block diagram of the total energy control is shown in Fig. 2.

4) Differential Energy Control in Each Phase-Leg: Derivation of the differential energy can be represented as

$$\frac{dW_{Cx}^{\Delta}}{dt} = \frac{1}{2}V_{\rm dc}i_x - 2v_x i_{Zx} - L\frac{d\left(i_{Zx}i_x\right)}{dt} - 2Ri_{Zx}i_x \approx p_{0Cx}^{\Delta} + p_{1Cx}^{\Delta} + p_{2Cx}^{\Delta}. \tag{21}$$

If only the dc component (I_{Zx}) of circulating current i_{Zx} is considered, then (21) can be simplified into

$$p_{1Cx}^{\Delta} = \left(\frac{1}{2}V_{\rm dc} - \omega L I_{Zx} - 2RI_{Zx}\right) I_x \sin\left(\omega t - \emptyset\right) - 2V_x I_{Zx} \sin\left(\omega t\right) \tag{22}$$

where p_{1Cx}^{Δ} is the fundamental component of $\frac{dW_{Cx}^{\Delta}}{dt}$. As (22) shows, the capacitor voltages in the upper and lower arms contain fundamental ripples with opposite phases. As a result, the capacitors should be large enough to absorb these low-frequency ripples.

Besides dc component, there might also be ac components in i_{Zx}. According to orthogonality of sine functions, only the fundamental frequency component of i_{Zx} can produce nonzero average power with v_x. This fundamental component of i_{Zx} and the resultant dc component of $\frac{dW_{Cx}^{\Delta}}{dt}$ are given in (23) and (24), respectively

$$i_{1Zx} = I_{1Zx}\sin\left(\omega t + \varphi_x\right) \approx p_{0Cx}^{\Delta} + p_{1Cx}^{\Delta} + p_{2Cx}^{\Delta} \tag{23}$$

$$p_{0Cx}^{\Delta} = -V_x I_{1Zx}\cos\varphi_x - RI_{Zx}I_x\cos\left(\emptyset + \varphi_x\right). \tag{24}$$

Once the energies in the upper/lower arms are unbalanced, p_{0Cx}^{Δ} (which is varied through $I_{1Zx}\cos\varphi_x$) can be used to rebalance these energies. Hence, $I_{1Zx}\cos\varphi_x$ can be selected as the output of energy balance or differential energy controller. The detailed control block is shown in Fig. 3. To minimize the amplitude of i_{1Zx}, φ_x is set to zero. Phase-locked loop is adopted to get the phase of ac voltage v_x.

5) Overall Control Structure: Based on the aforementioned analyses, an energy-based overall control structure for MMC operating as an inverter is presented in Fig. 4. The total energy control, differential energy control, circulating current control, and ac current control are all included. To simplify the computational burden, the capacitor voltages within one arm are supposed to be balanced, i.e.,

$$\begin{cases} W_{CPx} = \dfrac{1}{2}C\displaystyle\sum_{j=1}^{N} v_{CPxj}^2 \approx \dfrac{C}{2N}\left(\sum v_{CPx}\right)^2 \\ W_{CNx} = \dfrac{1}{2}C\displaystyle\sum_{j=1}^{N} v_{CNxj}^2 \approx \dfrac{C}{2N}\left(\sum v_{CNx}\right)^2 \end{cases} \tag{25}$$

The arm reference voltages can be derived from (3) and (5) as

$$\begin{cases} v_{Px} = v_{2x} + v_{1x} \\ v_{Nx} = v_{2x} - v_{1x} \end{cases} \tag{26}$$

In Fig. 4, the total energy controller and differential energy controller can be designed according to (18) and (24). The ac current controller and circulating current controller can be designed according to (4) and (7). Since low frequency harmonics exist in W_{Cx}^{Σ} and W_{Cx}^{Δ}, low-pass filters or controllers with low bandwidth should be adopted. To suppress the low-frequency harmonics in circulating currents, various circulating current control strategies as proposed in [19], [27], [28], can be easily embedded in this control structure. The red dotted-line box in Fig. 4 indicates the closed-loop current control in applications like grid-connected converters.

Large signal models are used in the energy-based control structure in Fig. 4, which guarantees large signal stability. However, if direct capacitor voltage control (i.e., voltage-based control) is needed, the structure can be easily modified as shown in Fig. 5. Voltage-based control is more intuitive, but small-signal linearized models have to be used and large signal stability is difficult to guarantee at the controller design stage.

III. Improved Modulation Method

PDPWM is one of the most important modulation methods for MMC, using one voltage reference and a group of level-shifted triangular carrier waves. However, powerful microcontroller chips with multiple modulation modules are required especially when the number of SMs is high, e.g., tens to hundreds. As a matter of fact, the reference is compared with only one carrier during each carrier period (T_{cr}) in PDPWM, as shown in Fig. 6(a). Therefore, theoretically only one voltage reference and one triangle carrier are necessary in each arm. This paper proposes an improved PDPWM, which requires much less hardware comparing units, but can provide excellent performance with inherent voltage balancing. The details of the improved modulation method are given as follows.

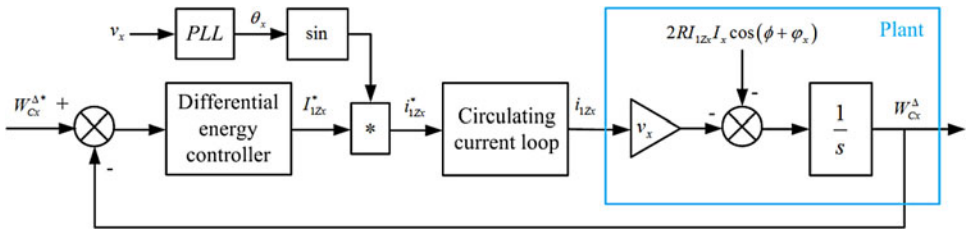


Fig. 3. Differential energy control.

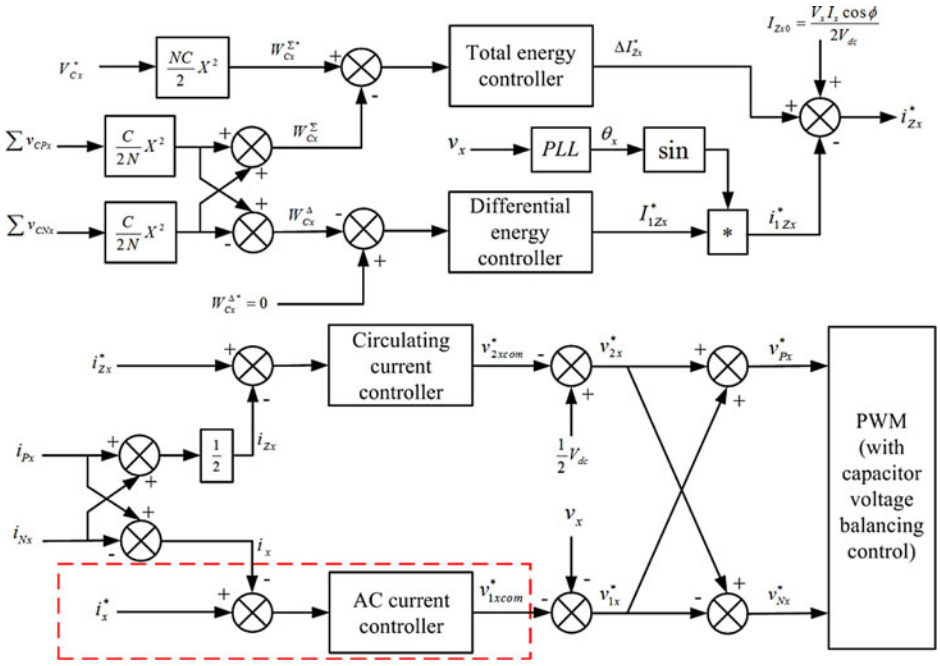


Fig. 4. Energy-based control structure of MMC operating as an inverter.

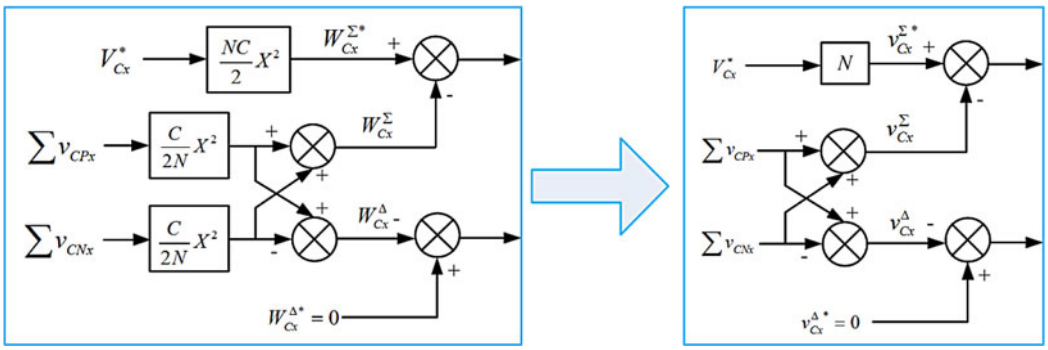


Fig. 5. Modification from energy-based control into voltage-based control.

Suppose the average value of the capacitor voltages in each arm is V_c, then the voltage reference v_r (from v_{Px}^* or v_{Nx}^* in Fig. 4) can be separated into an integral part and a fractional part, as shown in (27)

$$v_r = (n-1)\,V_c + dV_c \tag{27}$$

where $n = 1, 2, \ldots, N$, and $0 \le d \le 1$. That means, during each carrier period, only the nth SM operates in PWM mode (or switching mode), $(n-1)$ SMs (from 1 to $n-1$) at ON state, and $(N-n)$ SMs (from $n+1$ to N) at OFF state. Therefore, only one carrier is required for the modulation of the PWM-mode SM during each carrier period. As shown in Fig. 6(b), the output (v_p) of the PWM-mode SM is determined by comparing d with a double-edge triangular wave (v_{cr}), which has a maximal value of unity and a minimal value of zero. It is noted that in PDPWM, the carrier frequency $(f_{cr}$ or $1/T_{cr})$ is equal to the equivalent switching frequency $(Nf_{\rm sw})$ in one arm. The expected output $(v_{\rm pwm})$ of the modulation in one arm is a multilevel pulse waveform, which can be expressed as follows:

$$v_{\rm pwm} = (n-1)\,V_c + v_p. \tag{28}$$

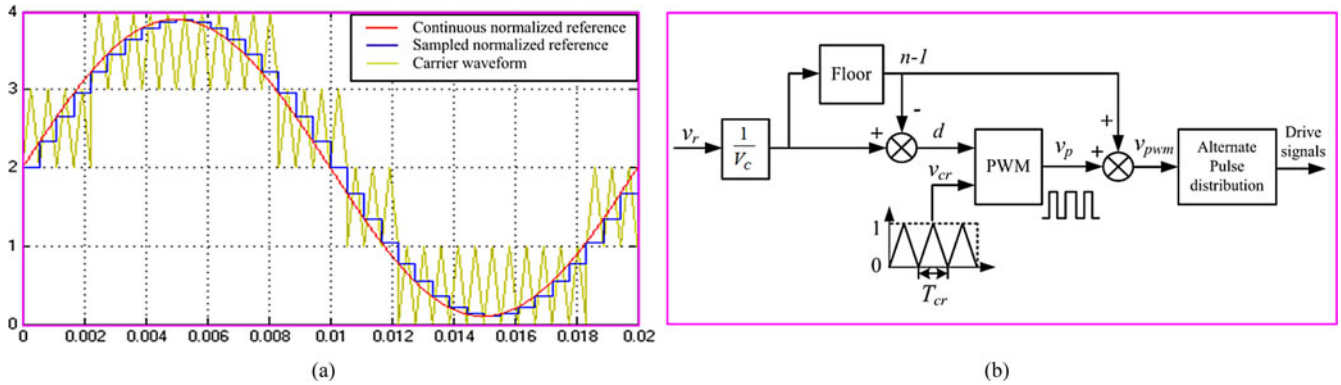


Fig. 6. Improved PDPWM with single reference and single carrier: (a) waveforms of reference and carrier; (b) implementation.

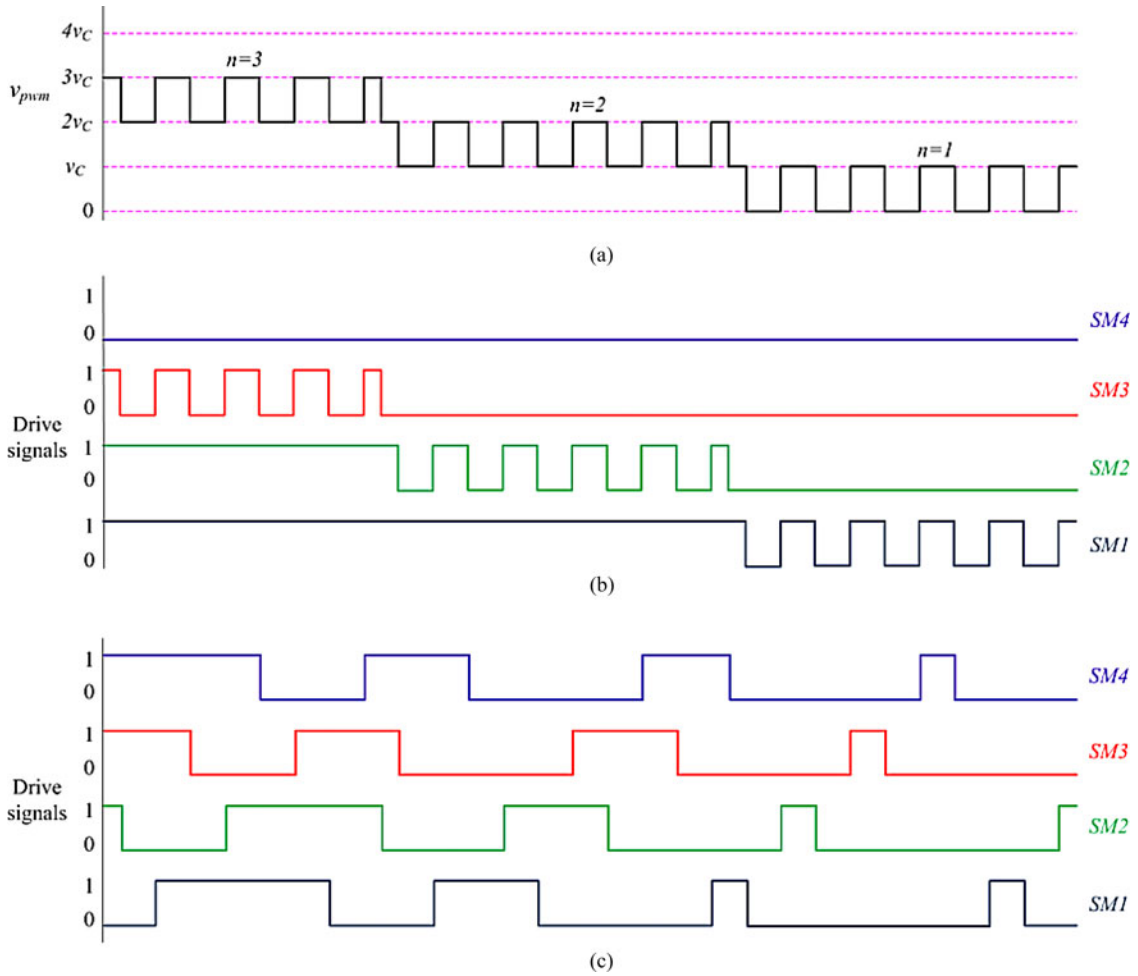


Fig. 7. Pulse distribution for PDPWM with four SMs in one arm: (a) expected pulse waveform; (b) direct pulse distribution; (c) proposed alternate pulse distribution.

After generating the pulse waveform v_{pwm} shown in Fig. 7(a), the next step is to distribute the pulse to all the SMs. In typical (or direct) pulse distribution method of PDPWM, the nth SM operating in PWM mode is directly assigned while the other SMs keep in ON or OFF state during each carrier period, as shown in Fig. 7(b). However, the direct pulse distribution method is likely to cause capacitor voltage imbalance because the powers flowing from/into different SMs are quite different.

To overcome this drawback, this paper proposes an alternate pulse distribution method. In Fig. 7(c), all the SMs within one arm alternately act every N ($N = 4$ here) triangular carrier periods. The same thing happens for the other arm in the same phase-leg, but with opposite states for the SMs due to the antiphase reference voltage. The algorithm of this alternate pulse distribution is shown in Fig. 8. With the alternate pulse distribution, each capacitor within one arm cycles through

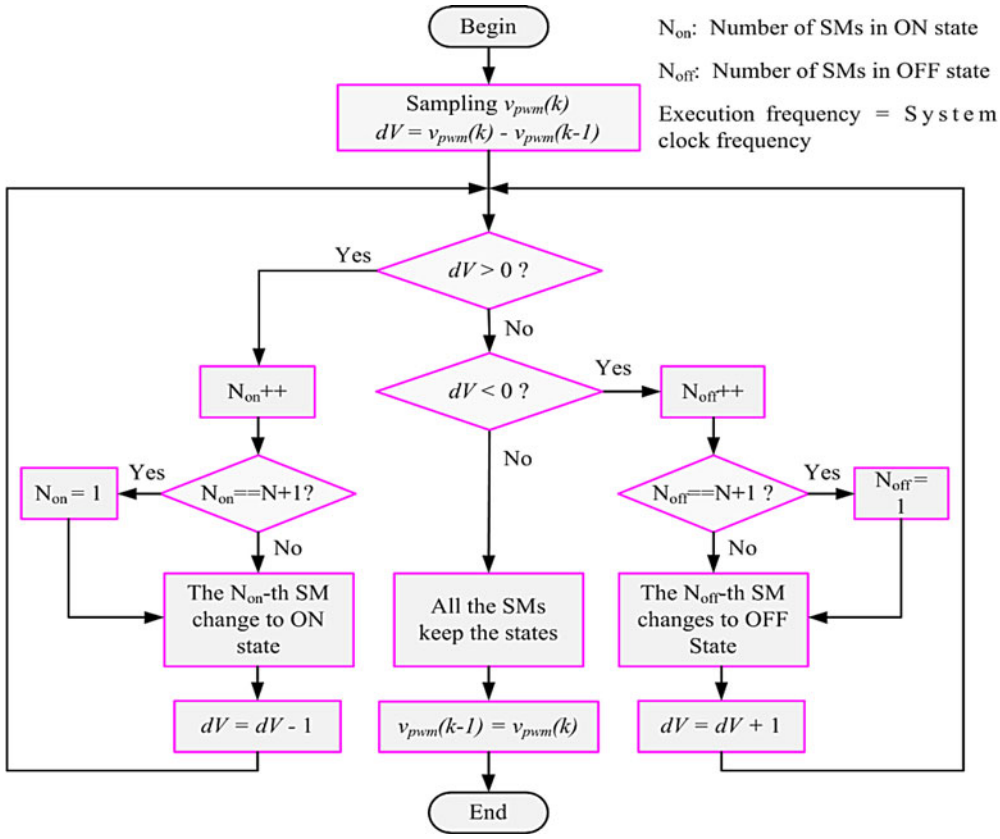


Fig. 8. Flowchart of alternate pulse distribution (implemented in an FPGA).

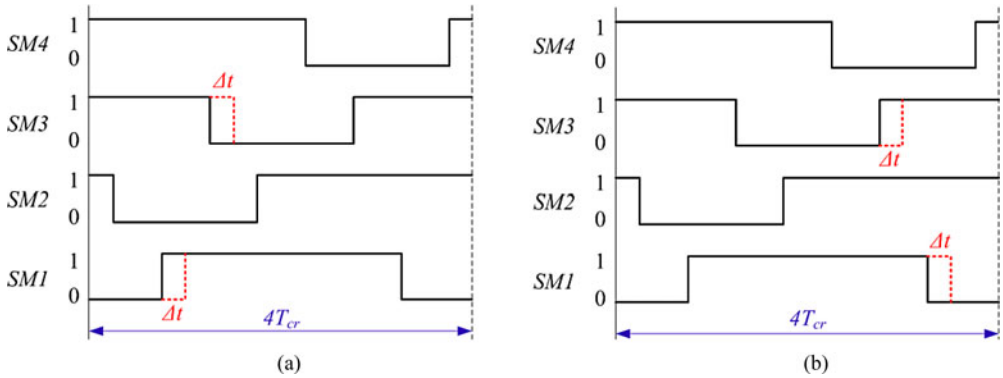


Fig. 9. Proposed capacitor voltage balancing for MMC: (a) negative arm current; (b) positive arm current.

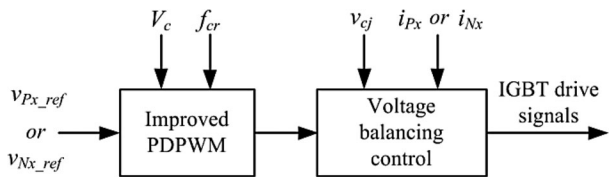


Fig. 10. Entire modulation and voltage balancing scheme.

charging/discharging and floating states once in every N carrier periods. This greatly improves the inherent voltage balancing capability, and therefore reduces the burden on the balancing control which will be discussed later. The algorithm in Fig. 10 can be easily realized with an FPGA. The complexity and hardware cost of this algorithm are low and do not increase with the number of SMs.

The proposed modulation method yields even distribution of switching frequency among power devices, which is similar to CPSPWM. Nonetheless, the hardware cost of the proposed method is much lower since it does not need separate PWM comparator for each SM.

IV. Voltage Balancing Control

The inherent voltage balancing capability of the improved PDPWM method is fairly good. However, some nonideal factors, e.g., differences in the SMs' losses and circuit parameters, can still disrupt the balance of capacitor voltages. This paper

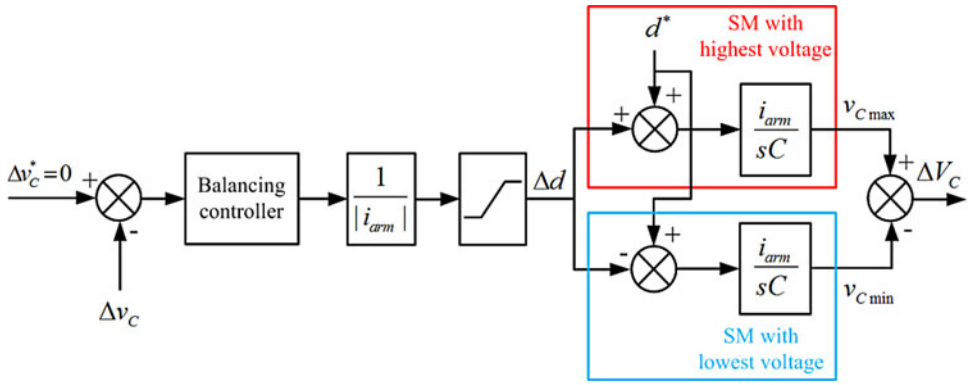


Fig. 11. Voltage balancing control within one arm.

TABLE I
COMPARISONS OF VOLTAGE BALANCING METHODS

Methods	Balancing accuracy	Dynamics	Switching frequency	Sorting	Cost	
					Hardware	Software
Distributed control [13]-[15]	Medium	Medium	Unchanged	No	High	High
Module selection [16]-[18]	High	Fast	Increased	Yes	Low	High
Reduced switching frequency [19]-[22]	Medium	Fast	Decreased	Yes	Low	High
Selective virtual loop mapping [20]	High	High	Increased	No	High	Low
Open loop control [21]	Medium	Slow	Unchanged	No	Low	Low
Method in [23]	Low	Slow	Unchanged	No	Low	High
Proposed method	High	Medium	Unchanged	No	Low	Low

TABLE II
PARAMETERS OF THE THREE-PHASE MMC FOR SIMULATION

Items	Values
Rated active power: P	2 MW
Rated reactive power: Q	0.5 MVar
Line voltage (rms): V_{LL}	6 kV
Line (or ac) frequency: f_1	50 Hz
DC-link voltage: V_{dc}	10 kV
Arm inductance: L	2 mH (3.6%)
Arm equivalent resistance: R	0.05 Ω
No. of SMs in each arm: N	4
SM capacitor: C	2 mF
Rated capacitor voltage: V_C	2.5 kV
Switching frequency: f_{sw}	2 kHz
Equivalent switching frequency in one arm: Nf_{sw}	8 kHz

presents a new voltage balancing control method based on the improved PDPWM, which does not need voltage sorting algorithm and does not cause extra switching actions.

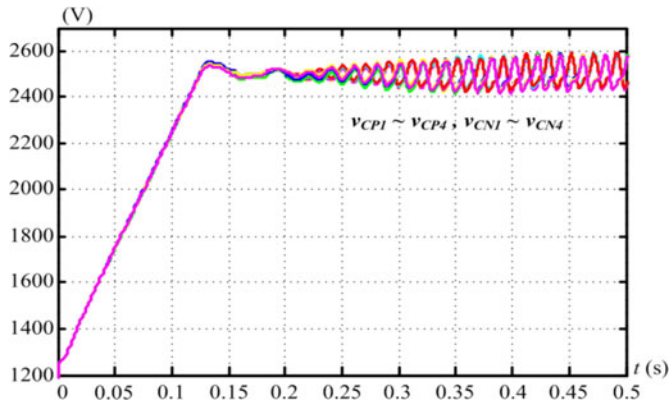


Fig. 12. Capacitor voltages during start-up.

A. Proposed Voltage Balancing Control Scheme

In the improved PDPWM, the imbalance among capacitor voltages develops slowly, therefore the balancing control needs not to be executed at the switching frequency (f_{cr}), and it needs not to adjust all the SMs. In this paper, the balancing action is only applied to the SMs with the highest and lowest voltage, and the control algorithm is executed at a low frequency (f_{cr}/N). To satisfy the charge balance, if arm current is positive, the pulse

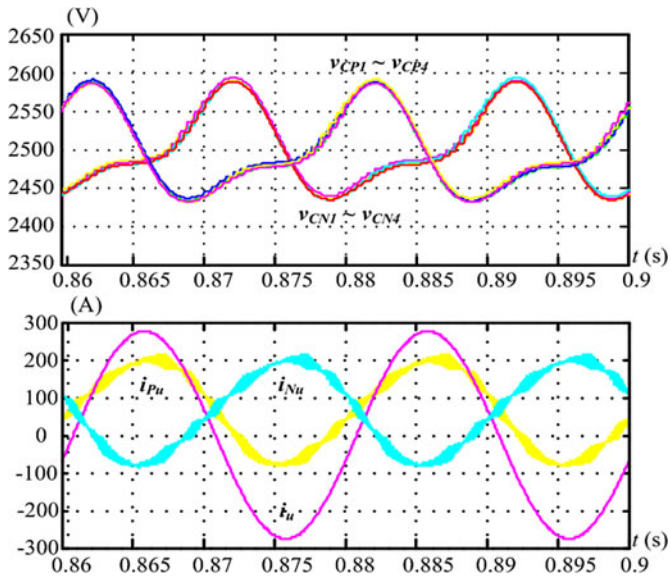


Fig. 13. Capacitor voltages, upper/lower arm currents, and ac current in steady state.

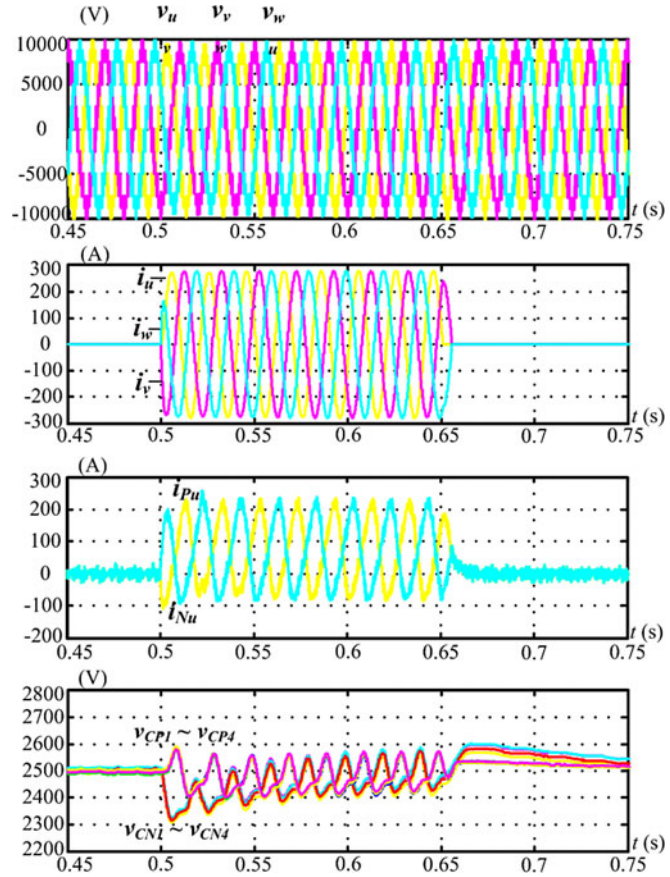


Fig. 14. Output voltages, output currents, arm currents, and capacitor voltages during sudden load changes.

width of the SM with highest voltage is reduced while the pulse width of the SM with lowest voltage is increased by the same amount. The opposite thing happens when the arm current is negative.

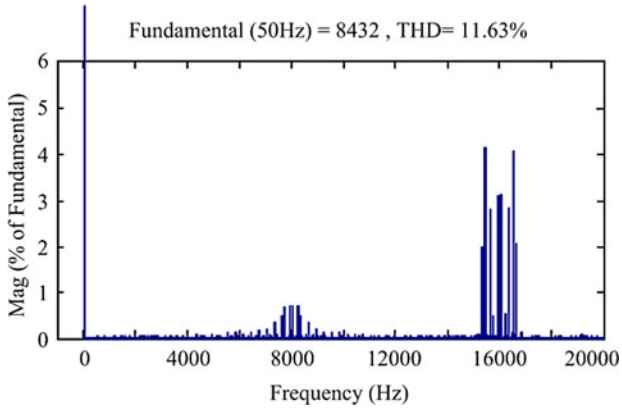


Fig. 15. Spectral analysis of simulated line voltage.

This scheme can be realized as follows. First, in each carrier period, the capacitor voltages are measured to find out the highest and lowest voltages. If the arm current is positive, the SM with the highest voltage is switched ON with a delay (Δt), while the SM with the lowest voltage is switched OFF with the same delay. If the arm current is negative, the SM with the highest voltage is switched OFF with a delay, while the SM with the lowest voltage is switched ON with the same delay. An example with $v_{C1} \leq v_{C2} \leq v_{C4} \leq v_{C3}$ is shown in Fig. 9, in which the red dotted-line denotes the modifications on the original PWM signal. The entire modulation and voltage balancing scheme is shown in Fig. 10.

B. Selection of Time Delay Δt

When the imbalance within one arm occurs, the average values of the capacitor voltages are different, but their low-frequency ripples vary with the same amplitude and in the same direction. The difference (Δv_C) between the highest voltage $(v_{C\max})$ and lowest voltage $(v_{C\min})$ is nearly constant, which should be zero when the voltage balancing is achieved. Therefore, Δv_C is used as the error and a simple P or PI controller is adopted to adjust the unbalance. Fig. 11 shows the control block diagram, where Δd is used for the computation of the time delay (Δt)

$$\Delta d = \Delta t / T_{cr}. \tag{29}$$

T_{cr} is the carrier period. Thanks to the improved modulation method, a low bandwidth of the balancing control system can be selected. The upper limit of Δd in Fig. 11 can also be set to a low value, e.g., 10%.

C. Discussion

Since the delays of the gating signals are the same, the volt-seconds of the arm voltages (v_{Px} and v_{Nx}) do not change during the time of NT_{cr}. Therefore, the proposed method will not affect the converter output voltage. Since the proposed balancing method only adds delays to the original gating signals, it does not cause unnecessary switching actions (which may occur with conventional module selection methods). Meanwhile,

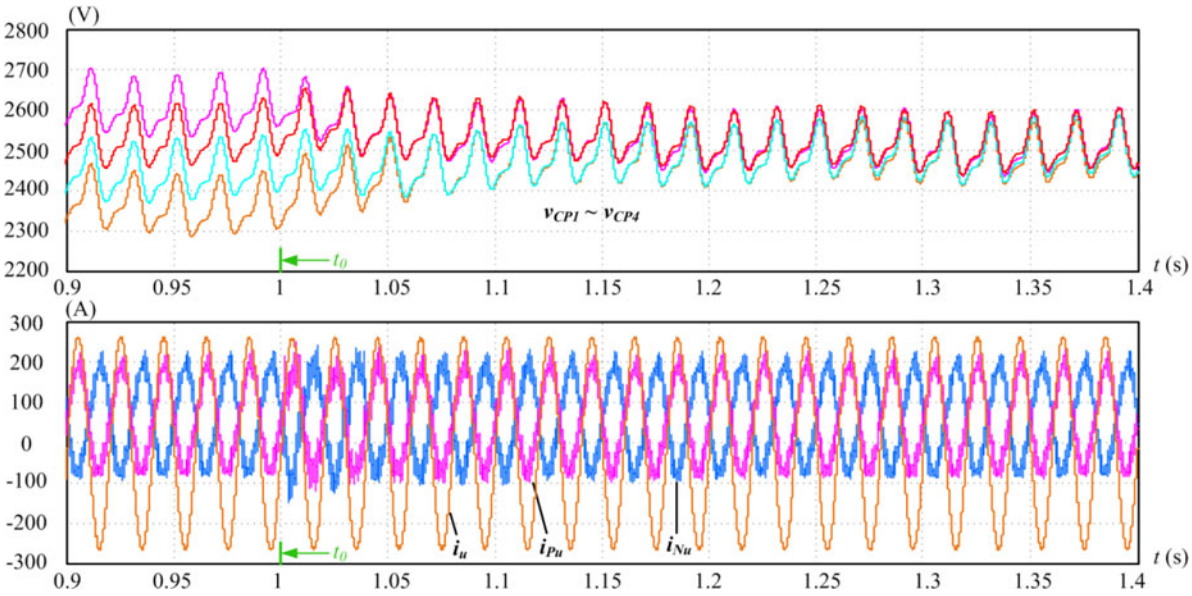


Fig. 16. Capacitor voltages, arm currents, and ac current with and without voltage balancing control.

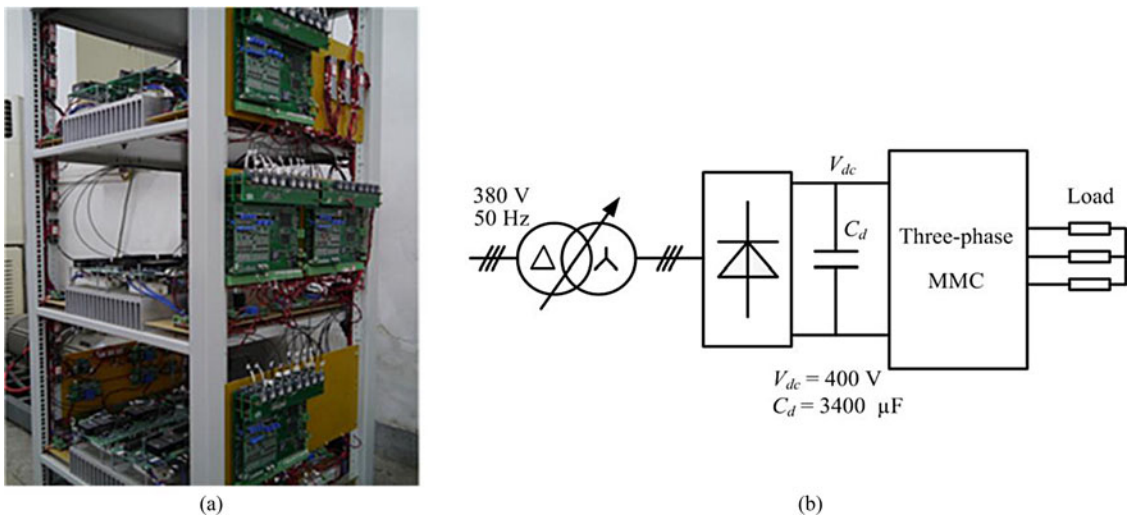


Fig. 17. (a) The experimental setup. (b) Configuration of the experimental system.

the method avoids the usage of a full sorting algorithm since it only needs to find out SMs with the highest and lowest voltages. Therefore, the computational burden is reduced, especially when the number of SMs is fairly high. Furthermore, compared with the method proposed in [13], higher balancing accuracy can be achieved, since the control error in the proposed method is a dc component while in [13] the errors contain low-frequency ripples.

A comparison of present voltage balancing methods and the proposed method, which encompasses a broad range of features, is presented in Table I. The comparison on cost is based on the assumption that the number of SMs within one arm is high.

V. Simulation Results

To verify the proposed control system, a three-phase MMC inverter with a resistor-inductor load is developed by MATLAB/Simulink software, and the parameters are summarized in Table II. PI controllers are used for total energy control, differential energy control, and circulating current control in the simulations and experiments.

To start the operation, the voltages of the SM capacitors are firstly charged to 1.25 kV ($V_{\rm dc}/2N$) via a precharging circuit. Then, it is charged to the rated value (2.5 kV) by total energy control under zero-output condition. During this process, the ripples in capacitor voltages are very low, as shown in Fig. 12. The low-frequency ripples gradually increase when the ac voltage and current ramp up to the rated values from 0.2 to 0.45 s.

Figs. 13 and 14 are the simulated waveforms in steady state and during transients. Fig. 13 shows the SM capacitor voltages, upper/lower arm currents, and ac current in phase u. It can be seen that all the capacitor voltages average 2.5 kV with roughly 150 V peak-to-peak ripple, indicating that the total energy control, differential energy control, and balancing control all work

TABLE III
PARAMETERS OF THE THREE-PHASE MMC FOR EXPERIMENT

Items	Values
Rated active power: P	3 kW
Line voltage (rms): V_{LL}	228 V
Line (or ac) frequency: f_l	50 Hz
DC-link voltage: V_{dc}	400 V
Arm inductance: L	4.62 mH
Arm equivalent resistance: R	0.1 Ω
No. of SMs in each arm: N	2
SM capacitor: C	560 μF
Rated capacitor voltage: V_C	200 V
Switching frequency: f_{sw}	2 kHz
Equivalent switching frequency in one arm: Nf_{sw}	4 kHz
Load resistor (Y-connected): R_L	24.5 Ω

well. Fig. 14 demonstrates the three-phase output voltages, upper/lower arm currents, and SM capacitor voltages during sudden load changes (the load is switched on at 0.5 s and switched off at 0.65 s). Fig. 15 presents the spectral analysis of output line voltage, which shows the dominant harmonics centered at 16 kHz ($2Nf_{\rm sw}$) as expected.

To highlight the effectiveness of the balancing control, a 10-kΩ resistor is parallel-connected to the capacitor of SM1 in phase u, and the balancing control is activated at $t = 1.0$ s. As shown in Fig. 16, there is significant imbalance before 1.0 s and the imbalance is quickly reduced to a negligible level after 1.0 s.

VI. EXPERIMENTAL RESULTS

A down-scaled prototype of three phase MMC inverter shown in Fig. 17(a) with resistive load is built for the experiments and the parameters are listed in Table III. The power devices are the BSM50GB60DLC IGBTs from Infineon. The dc-link voltage is generated from a three-phase diode rectifier connected to a three-phase autotransformer, as shown in Fig. 17(b). The proposed control and modulation methods are implemented with a TI TMS320F2812 DSP and an Altera EP1C12Q240I7 FPGA.

Fig. 18 shows the steady-state waveforms of phase u, where all the capacitor voltages are well balanced at 200 V with roughly 13 V peak-to-peak ripple. Figs. 19 and 20 are experimental waveforms of three-phase line voltages and currents during step load change. These experimental results show good dynamic performance of the MMC control system.

Fig. 21 gives the spectral analysis of the line voltage with and without load. In both cases, the dominant harmonics center at 8 kHz as expected. When the load is connected, the THD of the line voltage reduces drastically. This is because the smoothing inductors of the MMC inverter work as output filters only when load is connected.

Fig. 22 exhibits the indispensability of the differential energy control which helps balance the capacitor voltages of the upper and lower arms. The differential energy control is cut off at

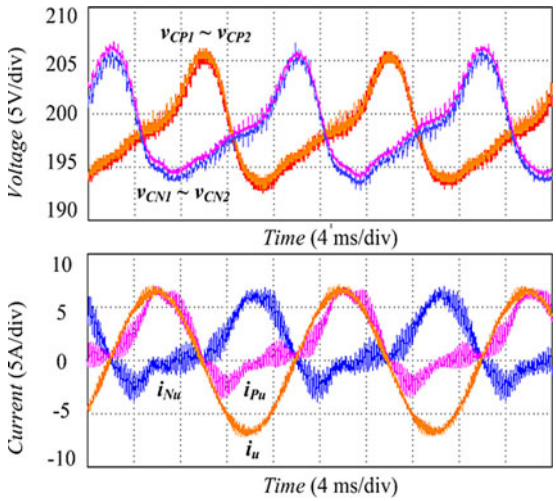


Fig. 18. Capacitor voltages, arm currents, and ac current in steady state.

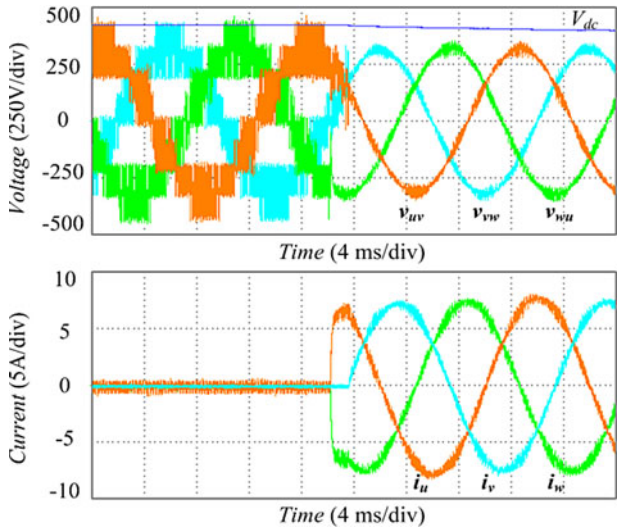


Fig. 19. Line voltages and currents with step increase of load.

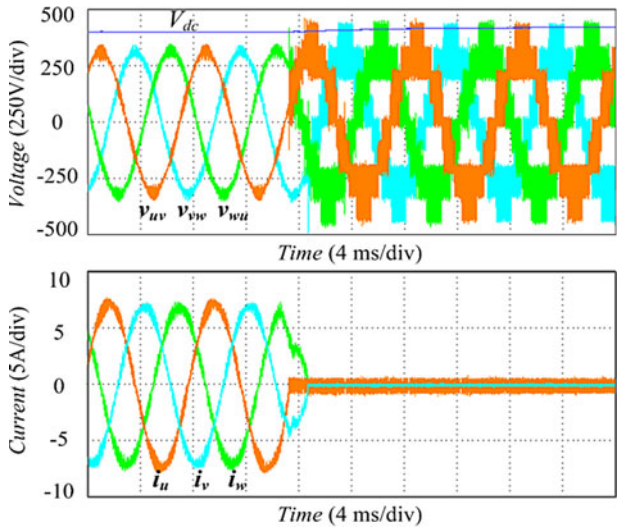


Fig. 20. Line voltages and currents with step decrease of load.

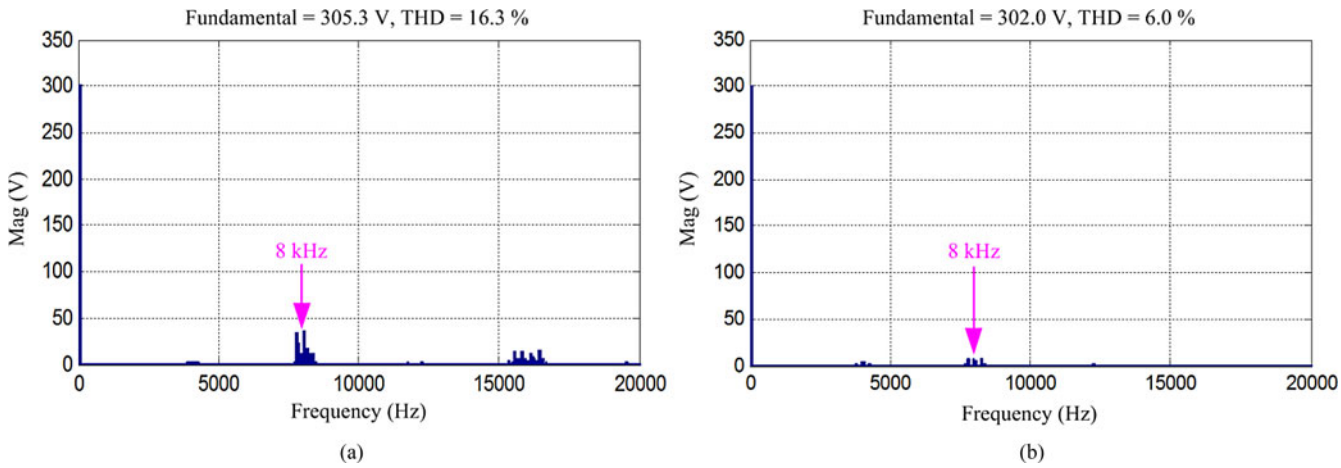


Fig. 21. Spectral analysis of line voltage (a) without load, (b) with load.

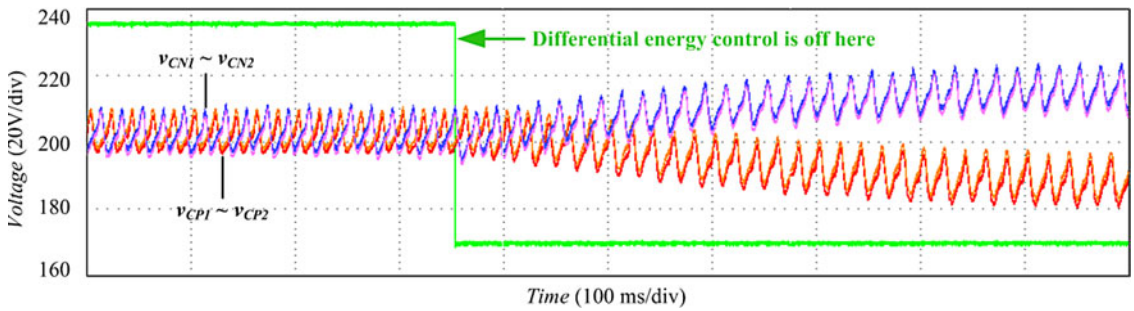


Fig. 22. Capacitor voltages, arm currents, and ac current with and without differential energy control.

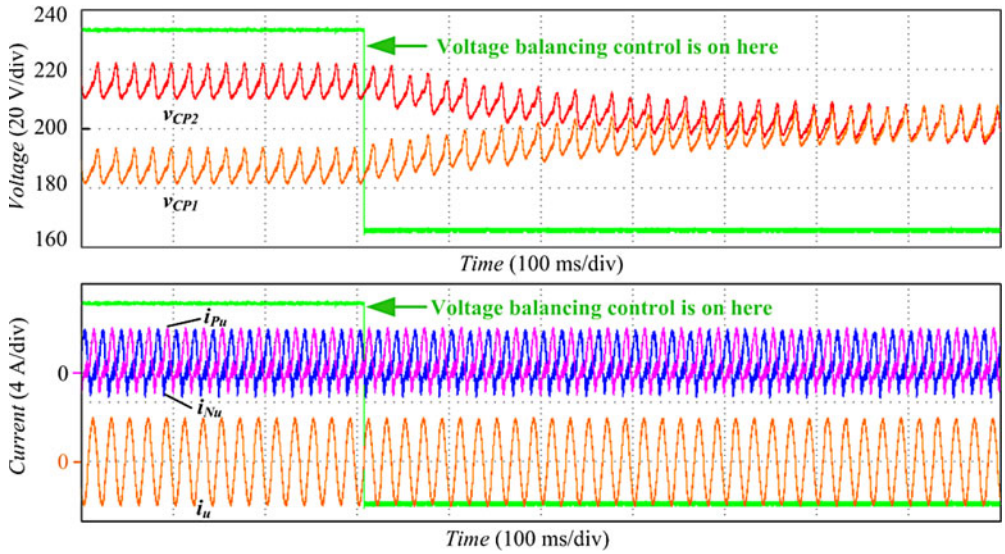


Fig. 23. Capacitor voltages, arm currents, and ac current with and without voltage balancing control.

0.45 s. Without differential energy control, the capacitor voltages in upper/lower arms are seen to deviate from each other significantly. Note that the capacitor voltages within one arm are still the same because the voltage balancing control within one arm is working.

Fig. 23 shows the dynamic performance of the voltage balancing control within one arm. To highlight the balancing ability of the method, a 4-kΩ resistor is paralleled to the capacitor of SM1 in phase u. Significant voltage imbalance can be observed in Fig. 23 before the balancing control is activated. Then, the imbalance quickly diminishes after the proposed balancing control is applied. The waveforms of upper/lower arm currents and ac current during the process show that the output power quality is not affected.

VII. Conclusion

A new voltage balancing control method in conjunction with an improved PDPWM method is proposed. The improved PDPWM method distributes the gating pulses alternately among the SMs within one arm every N (number of SMs within one arm) several carrier periods. The SM capacitor voltages can be well balanced without using a full voltage sorting algorithm and without causing unnecessary switching actions. Single reference and single carrier (for one arm) used in the modulation reduce the control hardware requirement. These features make the proposed balancing control method a more suitable solution for medium- and high-voltage applications, where the number of SMs in each arm can be fairly high. Except for some extreme cases where the SM switching frequency drops below 100 Hz (due to an excessively high SM numbers and/or a low MMC equivalent switching frequency), the performances of the improved modulation and balancing control are found to be satisfactory.

A general-purpose control structure is also proposed, which is adaptable for various control modes. It also features a balancing control between the upper and lower arms based upon proper differential energy control and circulating current control. Simulation and experimental results verified the good performances of the MMC system with the proposed methods.

References

[1] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[3] S. S. Fazel, S. Bernet, D. Krug, and K. Jalili, "Design and comparison of 4-kV neutral-point-clamped, flying-capacitor, and series-connected H-bridge multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1032–1040, Jul./Aug. 2007.

[4] J. Pou, R. Pindado, and D. Boroyevich, "Voltage-balance limits in four-level diode-clamped converters with passive front ends," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 190–196, Feb. 2005.

[5] S. B. Monge, S. Alepuz, J. Bordonau, and J. Peracaula, "Voltage balancing control of diode-clamped multilevel converters with passive front-ends," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1751–1758, Jul. 2008.

[6] B. P. McGrath and D. G. Holmes, "Enhanced voltage balancing of a flying capacitor multilevel converter using phase disposition (PD) modulation," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1933–1942, Jul. 2011.

[7] J. Wang and F. Z. Peng, "Unified power flow controller using the cascade multilevel inverter," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 1077–1084, Jul. 2004.

[8] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," presented at the IEEE Power Tech Conf., Bologna, Italy, 2003.

[9] M. Davles, M. Dommaschk, J. Dorn, J. Lang, D. Retzmann, and D. Soerangr, "HVDC Plus Basics and principle of operation," Siemens AG, 2011.

[10] K. Ilves, A. Antonopoulos, S. Norrga, and H.-P. Nee, "Steady-state analysis of interaction between harmonic components of arm and line quantities of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 57–68, Jan. 2012.

[11] H. P. Mohammadi and M. T. Bina, "A transformerless medium-voltage STATCOM topology based on extended modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1534–1545, May 2011.

[12] K. Ilves, S. Norrga, L. Harnefors, and H. P. Nee, "On energy storage requirements in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 77–88, Jan. 2014.

[13] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.

[14] M. Hagiwara and H. Akagi, "Control and analysis of modular multilevel cascade converter based on double-star chopper-cells (MMCC–DSCC)," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1649–1658, Jun. 2011.

[15] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3119–3130, Nov. 2011.

[16] K. Wang, Y. Li, Z. Zheng, and L. Xu, "Voltage balancing and fluctuation suppression methods of floating capacitors in a new modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1943–1954, May 2013.

[17] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2633–2642, Aug. 2010.

[18] Z. Li, P. Wang, H. Zhu, Z. Chu, and Y. Li, "An improved pulse width modulation method for chopper-cell-based multilevel inverters," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3472–3481, Aug. 2012.

[19] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel PWM Converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.

[20] J. Mei, B. Xiao, K. Shen, L. M. Tolbert, and J. Y. Zheng, "Modular multilevel inverter with new modulation method and its application to photovoltaic grid-connected generator," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5063–5073, Nov. 2013.

[21] K. Ilves, A. Antonopoulos, S. Norrga, and H.-P. Nee, "A new modulation method for the modular multilevel converter allowing fundamental switching frequency," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3482–3494, Aug. 2012.

[22] J. Qin and M. Saeedifard, "Reduced switching-frequency voltage-balancing strategies for modular multilevel HVDC converters," *IEEE Trans. Power Del.*, vol. 28, no. 4, pp. 2403–2410, Oct. 2013.

[23] F. Deng and Z. Chen, "A control method for voltage balancing in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 66–76, Jan. 2014.

[24] S. Allebrod, D. Schmitt, and R. Marquardt, "Control structure for modular multilevel converters," in *Proc. Power Convers. Intell. Motion Eur.*, Nuremberg, Germany, May 12–14, 2009, pp. 576–581.

[25] A. Antonopoulos, L. Ängquist, and H.-P. Nee, "On dynamics and voltage control of the modular multilevel converter," presented at the Eur. Power Electron., Barcelona, Spain, Sep. 2009.

[26] G. Bergna, E. Berne, P. Egrot, P. Lefranc, A. Arzandé, J.-C. Vannier, and M. Molinas, "An energy-based controller for HVDC modular multilevel converter in decoupled double synchronous reference frame for voltage oscillation reduction," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2360–2371, Jun. 2013.

[27] Z. Li, P. Wang, Z. Chu, H. Zhu, Y. Luo, and Y. Li, "An inner current suppressing method for Modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4873–4879, Nov. 2013.

[28] M. Zhang, L. Huang, W. Yao, and Z. Lu, "Circulating harmonic current elimination of a CPS-PWM-based modualr mulitlevel converter with a plug-in repetitive controller," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2083–2097, Apr. 2014.

Shengfang Fan (S'12) was born in Hubei, China, in 1985. He received the B.E. degree from the Huazhong University of Science and Technology, Wuhan, China, in 2009, where he is currently working toward the Ph.D. degree at the School of Electrical and Electronic Engineering.

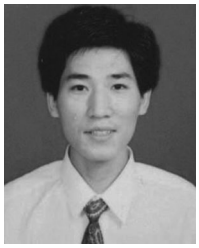
From December 2011 to November 2012, he was an Intern in Corporate Technology, Siemens Corporation, Princeton, NJ, USA. His research interests include design and control of power electronics systems, ac drives, high power factor rectifiers, and modular multilevel converters.

Kai Zhang was born in Henan Province, China. He received the B.E., M.E., and the Ph.D. degrees from the Huazhong University of Science and Technology (HUST), Wuhan, China, in 1993, 1996, and 2001, respectively.

He joined HUST as an Assistant Lecturer in 1996. He was a Visiting Scholar at the University of New Brunswick, Fredericton, NB, Canada, during 2004 to 2005. He was promoted to a Full Professor in 2006. He is the author of more than 40 technical papers. His research interests include uninterruptible power system, railway traction drives, modular multilevel converters, and electromagnetic compatibility techniques for power electronic systems.

Jian Xiong was born in Hubei Province, China. He received the B.E. degree from East China Shipbuilding Institute, Zhenjiang, China, in 1993, and the M.E. and Ph.D. degrees from the Huazhong University of Science and Technology (HUST), Wuhan, China, in 1996 and 1999, respectively.

He joined HUST as a Lecturer in 1999, where he was promoted to an Associate Professor in 2003. His research interests include uninterruptible power system, ac drives, switch-mode rectifiers, STATCOM, and the related control techniques.



Yaosuo Xue (M'03–SM'12) received the B.Sc. degree in electrical engineering from East China Jiaotong University, Nanchang, China, in 1991, and the M.Sc. degree in electrical engineering from the University of New Brunswick, Fredericton, NB, Canada, in 2004 where he is currently working toward the Ph.D. degree.

From 1991 to 2000, he was an Electrical Engineer and conducted research and design in high-speed electric railway in Electrification Research Division, Third Survey and Design Institute of the China's Ministry of Railways, where he has led the planning and design of traction power supply systems for several national key railway engineering, including Qinhuangdao–Shenyang Passenger Railway, the first de-facto high-speed railway in China. During 2005 to 2006, he worked in Capstone Turbine Corp. in California as a Lead Power Electronics and Systems Engineer developing advanced microturbine systems. Since 2009, he has been a Research Scientist and is currently the Research Project Manager at Corporate Technology, Siemens Corporation, Princeton, NJ, USA, where he co-founded the Siemens Corporate Technology's power electronics research group in USA. His current research interests include modular multilevel converters, energy buffering, and smart inverter controls as well as their applications for microgrids and grid integrations of renewable energy.