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An Improved DC-Link Voltage Control Strategy for Grid Connected Converters

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***Abstract*—This paper presents a robust control strategy to improve dc-link voltage control performances for Grid connected Converters (GcCs). The proposed control strategy is based on an adaptive PI controller and is aimed to ensure fast transient response, low dc-link voltage fluctuations, low grid current THD and good disturbance rejection after sudden changes of the active power drawn by the GcC. The proportional and integral gains of the considered adaptive PI controller are self-tuned so that they are well suited with regard to the operating point of the controlled system and/or its state. Several simulation and experimental results are presented to confirm and validate the effectiveness and feasibility of the proposed dc-link voltage control strategy.**

***Index Terms*—DC-link voltage control, adaptive PI controller, Grid connected Converters**

I. Introduction

Nowadays, power converters have an important role in a large scale of industrial applications since they allow efficient power transmission between the grid (on one side) and loads or energy sources (on the other side). The commonly used power converters topologies use a dc-link as an intermediate stage for the power conversion process in addition to a Grid connected Converter (GcC) and a filter based on passive (inductive and/or capacitive) elements. For example, this is the case of adjustable speed drives [1-2], renewable energy sources [3-4], active power filters [5-6], UPS systems [7] and back-to-back systems [2],[8]. Efficient dc-link voltage control is very important for such applications to reduce voltage fluctuations in the dc-link [9], which are mainly caused by random changes (particularly sudden and sever changes) in the power drawn by the GcC. When these fluctuations cross their limits, the protection devices are activated leading to a system shut-down [3],[9]. Thus, the control objectives pertaining to the dc-link voltage can be summarized in the following key points: 1) the voltage across the dc-link capacitor must be kept at a constant value by controlling the power flow in the AC side of the GcC so that two objectives are satisfied: the first one is the upkeep of the capacitor charge, while the second one is the supply of a load connected to the dc-link (for the rectifying mode case) or the transfer of the power provided by a DC source (for the inverting mode case), 2) the dc-link voltage fluctuations must be minimized, 3) the generation of high grid current harmonics must be prevented and 4) The deviation from the unity power factor operation caused by the grid current ripples must be prevented.

The most frequently used dc-link voltage controller is the PI controller [10],[11]. Different PI controller design techniques were described in literature. Among them, we can cite the pole zero cancellation method, the pole placement method and the optimum criterion method [8],[11]. For these methods, the PI controller is usually adjusted with respect to different constraints: C_1) stability; C_2) dynamic performances; C_3) disturbance rejection; and C_4) step responses with low overshoot [12]. In order to satisfy all these constraints, some research works presented the design of adaptive PI controllers [13-17]. Other ones combine between the benefits of the PI controller and the feed forward compensation method [18-20]. For that case, despite the excellent improvement of dynamic performances, such a method increases the coupling between the controlled dc-link voltage and the grid currents. Consequently, any noise or fast oscillation in the grid currents can create ripples at the output reference of the dc-link voltage controller. Other works have presented a Direct Power Control (DPC) combined with the boundary control [26] to improve the dynamic performances of the dc-link voltage. Compared to the conventional DPC, the dc-link voltage is considered for selection of the switching states through a switching table. As a result, no outer loop is needed and the dynamic performances are highly improved. However, this method results into a variable switching frequency, which is limited to the half of the used sampling period and which depends on the system parameters, dc-link voltage and ac-side voltage [23], [27]. So, the DPC combined with boundary control cannot be used for applications that require constant switching frequency, like the case of LCL-based GcCs since it will lead to resonance problems. Moreover, this control will lead to high grid current THD values during steady state operation if low mean switching frequency is achieved [23], [26].

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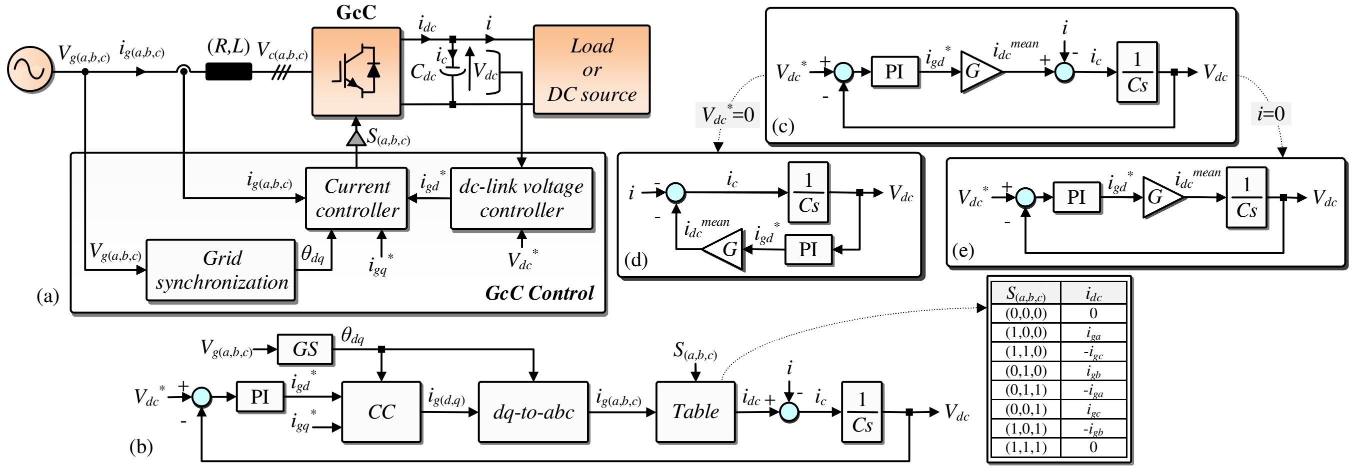

$S_{(a,b,c)}$	i_{dc}
(0,0,0)	0
(1,0,0)	i_{ga}
(1,1,0)	$-i_{gc}$
(0,1,0)	i_{gb}
(0,1,1)	$-i_{ga}$
(0,0,1)	i_{gc}
(1,0,1)	$-i_{gb}$
(1,1,1)	0

Fig. 1. (a) Commonly used control structure for Grid-connected Converters (b) Model of the dc-link voltage control system (c) Simplified model of the dc-link voltage control system (d) Equivalent simplified model when $V_{dc}^*=0$ (e) Equivalent simplified model when $i=0$

This paper proposes an efficient adaptive PI controller for the dc-link voltage control. The adaptive nature of the proposed PI controller guarantees the different control constraints $C_{(1..4)}$ mentioned in the previous paragraph in addition to the reduction of grid current THD during steady state operation, which is mainly caused by dc-link voltage controller's output signal. The proportional and integral gains of the considered adaptive PI controller are self-tuned according to the operating point of the controlled system and/or its state (*i.e.* transient or steady state). For that, a band around the dc-link voltage reference is defined. When the measured dc-link voltage is outside this band, the PI gains were selected constants so that a very good dynamic is achieved. Otherwise, the PI gains become variable so that the previously mentioned constrains remain still satisfied. Also, an anti-windup process is added in order to prevent large overshoot after step jumps of the dc-link voltage reference. The rest of the paper is organized as follow. Section II presents a simplified modeling, analysis and design of the dc-link voltage controller. Then, section III describes the proposed adaptive dc-link voltage controller. Accordingly, section IV shows and discusses the obtained experimental results with the proposed adaptive PI controller. Finally, section V summarizes the main conclusions of this work.

II. Modeling, Design and Analysis of the DC-Link Voltage Controller

A. *Modeling and design of the dc-link voltage controller*

The studied system is depicted on Fig.1.a, where L (respectively R) is the filter inductor (respectively the filter resistor); C is the capacitor of the dc-link; $V_{g(a,b,c)}$ refer to the components of the grid voltage vector in the natural reference frame; $i_{g(a,b,c)}$ refer to the components of the grid current vector in the natural reference frame; $S_{(a,b,c)}$ are the GcC switching states; V_{dc} is the dc-link voltage; V_{dc}^* is the dc-link voltage reference; i_{dc} is the current coming out from the power converter; i_c is the current flowing into the capacitor C; i is the current consumed/generated by the load/the DC source connected to the dc-link; and $i_{g(d,q)}^*$ are the d and q components of the grid current reference in the synchronous reference frame (d,q), where the d axis is linked to the grid voltage vector. Fig.1.a shows also that the control structure of a GcC includes three main functions: the grid synchronization [21], the current controller [22] and the dc-link voltage controller [11]. Fig.1.b shows the model of the dc-link voltage control system. In this figure, *GS* and CC stand for grid synchronization and current controller, respectively. It can be noted that the dc-link voltage control is not in the form of a LTI system. This is mainly due to nonlinearities introduced by the i_{dc} table that computes i_{dc} current based on grid currents $i_{g(a,b,c)}$ and applied switching signals $S_{(a,b,c)}$. To simplify the model, the relationship between the mean value of i_{dc} (i_{dc}^{mean}) and i_{gd}^* currents is firstly determined. This relationship is deduced according to equation (1) [20]. In this equation, P_{AC} is the active power fed in the AC side of the GcC, V_{gm} is the magnitude of the phase voltage, i_{gd} is the d component of the grid current and P_{DC} is the active power fed in the DC side of the GcC. Supposing that $V_{dc}\approx V_{dc}^*$ and neglecting the power losses on the GcC and on the internal resistor of the inductive filter ($P_{AC}\approx P_{DC}$), the relationship between i_{dc}^{mean} and i_{gd}^* currents can be deduced as shown in equation (1).

$$\left.\begin{array}{l} P_{AC}=\frac{3}{2}V_{gm}i_{gd}\approx\frac{3}{2}V_{gm}i^*_{gd} \\ P_{DC}=V_{dc}i_{dc}^{mean} \end{array}\right\}\rightarrow i_{dc}^{mean}\approx\underbrace{\frac{3}{2}\frac{V_{gm}}{V^*_{dc}}}_{G}i^*_{gd}=Gi^*_{gd} \quad (1)$$

For a simplest, but reasonably accurate modeling of the dc-link voltage control, the simplified model given by Fig.1.c is considered. This simplified model is based the following assumptions: 1) the dynamic of *CC* loop is very fast with regard to that of the dc-link voltage control loop and 2) the nonlinearities are neglected. According to Fig.1.c, the dc-link voltage controller has two inputs: 1) the dc-link voltage reference V_{dc}^* and 2) the input current i. To study the dc-link voltage control loop, the superposition method is considered. Using this method and supposing that the PI controller transfer function is equal to (K_{pdc}+K_{idc}/s), two systems are derived from Fig.1.c. For the first system (Fig.1.d and equation (2)), i is neglected, while V_{dc}^* is considered as an input. For the second system (Fig.1.e and equation (3)), i is considered as an input, while V_{dc}^* is neglected.

$$\frac{V_{dc}}{V_{dc}^*} = \frac{\frac{GK_{pdc}}{C}s + \frac{GK_{idc}}{C}}{s^2 + \frac{GK_{pdc}}{C}s + \frac{GK_{idc}}{C}} = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (2)$$

$$\frac{V_{dc}}{i} = \frac{-\frac{1}{C}s}{s^2 + \frac{GK_{pdc}}{C}s + \frac{GK_{idc}}{C}} = \frac{-\frac{1}{C}s}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (3)$$

Identifying denominators of (2) and (3), we deduce that $2\xi\omega_n = GK_{pdc}/C$ and $\omega_n^2 = GK_{idc}/C$, where ξ is the damping ratio and ω_n is the natural frequency of oscillation. The poles $p_{(1,2)}$ of the transfer functions given by (2) and (3) are equal to $-\xi\omega_n \pm j\omega_n\sqrt{(1-\xi^2)}$ for $0\leq\xi\leq1$. So, the system stability is guarantee whenever (4) is verified.

$$(\omega_n > 0 \quad and \quad \xi > 0) \rightarrow (K_{pdc} > 0 \quad and \quad K_{idc} > 0) \quad (4)$$

The standard PI controller can be designed using the pole placement method as in (5).

$$K_{pdc} = f(\xi, \omega_n) = \frac{2C\xi\omega_n}{G} \; and \; K_{idc} = f(\omega_n) = \frac{C\omega_n^2}{G} \quad (5)$$

B. Analysis of the dc-link voltage controller

- *Analysis of the dynamic response to a step jump of* V_{dc}^*

Based on equation (2), when a step jump is applied to the dc-link voltage reference value V_{dc}^*, the response of the dc-link voltage V_{dc} (initially equal to V_{dc}^{init}) is expressed according to (6) (with $\Phi = \cos^{-1}(\xi)$).

$$V_{dc}(t) = V_{dc}^{init} + (1 + \frac{2\xi}{\sqrt{1-\xi^2}} e^{-\xi\omega_n t} \sin(\omega_n \sqrt{1-\xi^2}\, t) - \frac{1}{\sqrt{1-\xi^2}} e^{-\xi\omega_n t} \sin(\omega_n \sqrt{1-\xi^2}\, t + \Phi))(V_{dc}^* - V_{dc}^{init}) \quad (6)$$

The peak time t_{peak} and the maximum overshoot value M_o of the dc-link voltage are deduced by solving ($dV_{dc}(t)/dt=0$ for equation (6)) and are given by equation (7).

$$t_{peak} = \frac{F_1(\xi)}{\omega_n} \; and \; M_o = V_{dc}(t_{peak}) - V_{dc}^* = F_2(\xi)(V_{dc}^* - V_{dc}^{init}) \quad (7)$$

$$F_1(\xi) = \frac{1}{\sqrt{1-\xi^2}} tg^{-1}\left(\frac{2\xi + \frac{\xi}{\sqrt{1-\xi^2}}\sin(\Phi) - \cos(\Phi)}{-\frac{2\xi^2}{\sqrt{1-\xi^2}} + \frac{\xi}{\sqrt{1-\xi^2}}\cos(\Phi) + \sin(\Phi)}\right)$$

$$F_2(\xi) = \frac{e^{-\xi F_1(\xi)}}{\sqrt{1-\xi^2}} (2\xi \sin(\sqrt{1-\xi^2}\, F_1(\xi)) - \sin(\sqrt{1-\xi^2}\, F_1(\xi) + \Phi))$$

According to equation (7), for a fixed value of ξ and after step jumps of the dc-link voltage reference V_{dc}^*, better dynamic performances and shorter transient times are obtained when ω_n increases. However, ω_n have no effect on the obtained maximum overshoot value M_o, which depends only on the selected value for the damping ratio ξ.

- *Analysis of the dynamic response to a step jump of i*

In the following, we suppose that the maximum active power P_{max} generated/consumed by the DC source/Load connected to the dc-bus is known. Consequently, the maximum value $I_{\max}$ of the input current i is equal to $I_{\max}=P_{max}/V_{dc}^*$. Note that technical literature traditionally neglects the instantaneous power of the L filters since it is constant during steady state operation for the case of three-phase GcCs. However, in rectifying mode and according to [30], the increase of the maximum value I_{max} will result in variation in the instantaneous power of the L filters and can lead to instability problems. That's why, the maximum current $I_{\max}$ is supposed lower than a limit current that can cause unstable operation of the system. Based on equation (3), the response to a step jump of the input current i from 0 to $I_{\max}$ is expressed as follows

$$V_{dc}(t) = V_{dc}^* - \frac{I_{\max}}{C\omega_n\sqrt{(1-\xi^2)}} e^{-\xi\omega_n t} \sin(\omega_n \sqrt{1-\xi^2}\, t) \quad (8)$$

The peak time t_p, after a step jump of the input current i, can be computed by solving ($dV_{dc}(t)/dt=0$ for equation (8)). The response time t_r (necessary for V_{dc} to reach again its reference V_{dc}^*) can be approximately deduced from (8). The times t_p and t_r and the maximum overshoot value M_p are expressed according to (9).

$$\begin{cases} t_p = \underbrace{\frac{1}{\omega_n}\frac{1}{\sqrt{1-\xi^2}} tg^{-1}(\frac{\sqrt{1-\xi^2}}{\xi})}_{F3(\xi)} = \frac{F_3(\xi)}{\omega_n} \\ t_r = \frac{1}{\omega_n}\underbrace{\frac{\pi}{\sqrt{1-\xi^2}}}_{F4(\xi)} = \frac{F_4(\xi)}{\omega_n} \\ M_p = V_{dc}(t_p) - V_{dc}^* = -F_5(\xi)\frac{I_{\max}}{\omega_n} \\ F_5(\xi) = \frac{1}{C\sqrt{1-\xi^2}} e^{-\xi F_3(\xi)} \sin(\sqrt{1-\xi^2}\, F_3(\xi)) \end{cases} \quad (9)$$

According to equation (9), for a fixed value of ξ, better dynamic performances and lower maximum overshoot value M_p are obtained after step jumps of input current i when ω_n increases.

C. Analysis of the grid current harmonics

To derive the relationship between the output current harmonics and the selected (ξ,ω_n) values, it shall be noticed that the grid current harmonics are affected by the ripples that may exist in the dc-link voltage controller output signal. These ripples are the result of the oscillating nature of the i_{dc} current. To simplify the study, let consider the case when the GcC operates with a constant switching frequency f_c. For that case, and according to [28], the dc-link current can be expressed according to equation (10).

$$i_{dc} = \underbrace{\frac{3}{4} m I_{gm} \cos(\Phi_1)}_{idc\ mean\ value} + \underbrace{(... + I_{\omega c} \cos(\omega_c t - 3\omega t + \Phi^1_{\omega c})}_{HF} \\ \underbrace{+ I_{\omega c} \cos(\omega_c t + 3\omega t + \Phi^2_{\omega c}) + ... + I_{2\omega c} \cos(2\omega_c t) + ...)}_{HF} \quad (10)$$

Where Φ_1, $\Phi_{\omega c}^1$ and $\Phi_{\omega c}^2$ are constant phase angles, m is the modulation index, $\omega=2\pi f=2\pi 50$ rad/s is the frequency of the grid currents, $\omega_c=2\pi f_c$ is the switching frequency, I_{gm} is the grid current magnitude, $I_{\omega c}$ and $I_{2\omega c}$ are the magnitudes of the main harmonic components (*i.e.* for the frequencies equal to $\omega_c \pm 3\omega$ and $2\omega_c$, respectively). Note that $I_{\omega c}$ and $I_{2\omega c}$ are proportional to the grid current magnitude I_{gm} with a coefficient that depends on the used modulation index m [28]. The pulsating current i_{dc} passes through the $1/(Cs)$ bloc to create the bus-voltage ripples. The main dc-link voltage ripples are then equal to

$$\tilde{V}_{dc} = \frac{I_{\omega c}}{C(j(\omega_c - 3\omega))} + \frac{I_{\omega c}}{C(j(\omega_c + 3\omega))} + \frac{I_{2\omega c}}{C(j2\omega_c)} \quad (11)$$

The magnitude of the dc-link current ripples on the PI controller output signal can be deduced from (11) as follows

$$\left|\tilde{i}_{dc}\right| = \frac{I_{\omega c}}{C}\left|\frac{1}{j(\omega_c - 3\omega)}\right| \times \left|K_{pdc} + \frac{K_{idc}}{j(\omega_c - 3\omega)}\right| \\ + \frac{I_{\omega c}}{C}\left|\frac{1}{j(\omega_c + 3\omega)}\right| \times \left|K_{pdc} + \frac{K_{idc}}{j(\omega_c + 3\omega)}\right| \\ + \frac{I_{2\omega c}}{C}\left|\frac{1}{j(2\omega_c)}\right| \times \left|K_{pdc} + \frac{K_{idc}}{j(2\omega_c)}\right| \quad (12)$$

A *normalized current ripple ratio* NCRR is defined and computed according to (13).

$$NCCR = \frac{\left|\tilde{i}_{dc}\right|}{I_{gm}} = \underbrace{\frac{I_{2\omega c}}{C I_{gm}} \frac{1}{(2\omega_c)^2} \times \sqrt{(2\omega_c)^2 K_{pdc}^2 + K_{idc}^2}}_{NCCR3} \\ \underbrace{+ \frac{I_{\omega c}}{C I_{gm}} \frac{1}{(\omega_c + 3\omega)^2} \times \sqrt{(\omega_c + 3\omega)^2 K_{pdc}^2 + K_{idc}^2}}_{NCCR2} \\ \underbrace{+ \frac{I_{\omega c}}{C I_{gm}} \frac{1}{(\omega_c - 3\omega)^2} \times \sqrt{(\omega_c - 3\omega)^2 K_{pdc}^2 + K_{idc}^2}}_{NCCR1} \quad (13)$$

Given that $I_{\omega c}$ and $I_{2\omega c}$ are proportional to the grid current magnitude I_{gm} [28] (with a coefficient that depends on the applied modulation index m), the NCCR depends on the used capacitor, the used switching frequency, the used modulation index m and the selected gains K_{pdc} and K_{idc} for the PI controller. The ripples around the switching frequency in the *dq* synchronous reference frame (*i.e.* respectively (f_c-3f), (f_c+3f) and 2f_c) become respectively (f_c-2f), (f_c+4f) and (2f_c+f) ripples in the natural reference frame. Assuming that $H_{cc}(s)$ is the closed-loop transfer function of the internal current control loop, the grid current will have harmonic content with a magnitude equal to NCCR1×$|H_{cc}(j(\omega_c-2\omega))|$+NCCR2× $|H_{cc}(j(\omega_c+4\omega))|$ + NCCR3×$|H_{cc}(j(2\omega_c+\omega))|$. This harmonic content will influence the grid current THD especially for low dc bus capacitor values, low switching frequency values and high selected K_{pdc} and K_{idc} gains (when ω_n increases). For the case of variable switching frequency, it is difficult to derive the main harmonic content of the dc-link voltage. However, for a given main harmonic content, the grid current THD is influenced in the same manner as the case of a constant switching frequency operation.

III. Proposed adaptive PI controller

A. Design of the adaptive PI controller

The discrete-time model of the proposed adaptive PI controller is given by equation (14). In this equation, the proportional and integral gains ($\check{K}_{pdc}$, $\check{K}_{pdc}$) are determined using an adaptive process, which is aimed to minimize the dc-link voltage transients (*i.e.* during transient states) and the grid current THD (*i.e.* during steady states). To avoid large overshoots of the bus voltage, especially after step jumps of the dc-link voltage reference V_{dc}^*, an anti-windup correction [24] was added.

$$\begin{cases} u[k] = \tilde{K}_{pdc}\Delta V_{dc}[k] + s[k] \\ s[k] = s[k-1] + \tilde{K}_{idc} T_s \Delta V_{dc}[k] \underbrace{-K_c u_{sat}[k-1]}_{Anti-windup\ correction} \end{cases} \\ (Sat)\begin{cases} if\ (u[k] \succ I_{g\max}) \Rightarrow (i_{gd}^*[k] = I_{g\max}) \\ elsif\ (u[k] \prec -I_{g\max}) \Rightarrow (i_{gd}^*[k] = -I_{g\max}) \\ else\ (i_{gd}^*[k] = u[k]) \end{cases} \quad (14) \\ if\ u[k] \neq i_{gd}^*[k] \Rightarrow u_{sat}[k] = u[k]\ else\ u_{sat}[k] = 0$$

where k is the k^{th} sampling period, i_{gd}^* is the grid current reference available at the saturation output (*Sat*), ΔV_{dc} is the dc-link voltage error, T_s is the sampling period, $I_{g\max}$ is the maximum tolerable grid current value, u_{sat} is the anti-windup term and K_c is the anti-windup gain. In this work, K_c was set to 0.02. Notice, that lower K_c values will not efficiently eliminate dc-link voltage overshoots, while higher K_c values will affect the dynamic of the dc-link voltage response.

For the design of the adaptive PI controller, the damping ratio ξ was firstly selected taking into account the following constraints: 1) Very small damping ratio (close to zero) will result in oscillatory response and 2) Very high damping ratio will result in over damped system that can affect dynamic performances. A good compromise between the above mentioned constraints seems to be a damping ratio ξ between 0.7 and 1. In the following and in order to simplify the study, the damping ratio ξ is supposed constant and equal to 0.7. Fig.2.a presents the block diagram of the proposed adaptive PI controller. As shown in this figure, the PI gains ($\check{K}_{pdc}$, $\check{K}_{pdc}$) are continuously updated according to the absolute value of the dc-link voltage error $|\Delta V_{dc}|$. A band value is defined around the dc-link voltage reference V_{dc}^* as shown in Fig.2.c. This band is equal to $2G_{dc}V_{dc}^*$, where G_{dc} is the half of the ratio between the band value and the dc-link voltage reference.

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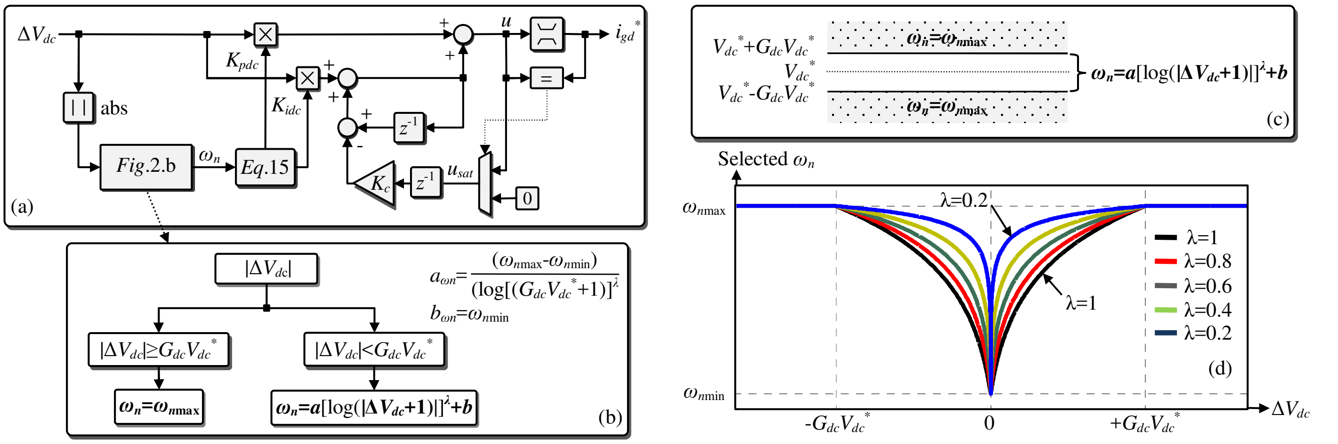

Fig. 2. (a) Adaptive anti-windup PI controller scheme (b) Computation process of the ω_n value (c-d) selected ω_n value according to ΔV_{dc}

The values of the higher and lower band limits are equal to $V_{dc}^*+G_{dc}V_{dc}^*$ and $V_{dc}^*-G_{dc}V_{dc}^*$, respectively. Outside the band, especially during startup or after step changes of the dc-link voltage reference V_{dc}^*, the natural frequency ω_n is selected equal to ω_{nmax}. In this case, the controller is employed as a standard PI with an anti-windup action. Inside the band, the ω_n value depends on the magnitude of the dc-link voltage error $|\Delta V_{dc}|$ and is selected according to the function given by equation (15). The main purpose of this function is to increase the selected ω_n value when the magnitude of the dc-link voltage error $|\Delta V_{dc}|$ increases during transient states. Conversely, during steady states, when $|\Delta V_{dc}|$ is close zero, the selected ω_n value must be approximately equal to $\omega_{n\min}$ to lead to a low grid current THD.

$$\begin{cases}\omega_n = a\left[\log(|\Delta V_{dc}|+1)\right]^{\lambda}+b \;\; if\; |\Delta V_{dc}| \le G_{dc}V_{dc}^* \\ \omega_n = \omega_{n\max} \;\; if\; |\Delta V_{dc}| \succ G_{dc}V_{dc}^* \end{cases} \quad (15)$$
$$\text{where } (0<\lambda\le 1, a=\frac{(\omega_{n\max}-\omega_{n\min})}{\left[\log(G_{dc}V_{dc}^*+1)\right]^{\lambda}}, b=\omega_{n\min})$$

The tuning of the adaptive PI parameters is detailed in the following

- *How to set the parameter* G_{dc} ?

The voltage rating of the dc-link voltage capacitor and GcC power switches is computed under dynamic conditions with an appropriate safety factor. In general, 10% overshoot of the dc-link voltage is considered under dynamic conditions. To this purpose, the G_{dc} gain (defined as the half of the ratio between the band value and V_{dc}^*) is chosen so that the dc-link voltage fluctuations remain lower than $10\%V_{dc}^*$, even after sudden and severe changes of the input current i. This means that, after a step jump of the input current i equal to its maximum value $\pm I_{\max}$, the dc-link voltage V_{dc} must remain inside the band $\pm G_{dc}V_{dc}^*$ around the dc-link voltage reference V_{dc}^*.

- *How to set the parameter* $\omega_{n\max}$?

As mentioned previously, the dynamic of the *CC* loop is assumed very fast with regard to that of the dc-link voltage control loop. The time constant τ_v of the dc-link voltage control loop is equal to $1/Re(p_{(1,2)})=1/(\xi\omega_n)$. Assuming that τ_i is the time constant of the *CC* loop, the time constant τ_v must be greater than $10\tau_i$. In this work, the time constant of the used CC loop τ_i is lower than 1ms. In order to achieve a time constant τ_v greater than 10ms, the ω_n value must be lower than a maximum value $\omega_{n\max}$ equal to $1/(\xi*10\text{ms})$. So, the $\omega_{n\max}$ value is selected equal to 142.86 rad/s=2π22.73 rad/s.

- *How to set the parameter* $\omega_{n\min}$?

The $\omega_{n\min}$ value can be determined so that the response time t_r (given by equation (9)) do not exceed a tolerable limit, even after maximum power load connection/disconnection. In this work the tolerable limit of t_r is set 10 times the grid period (t_r=10*20ms=200ms). For a ξ value set to 0.7 and based on equation (9), ω_{nmin} is equal to 21.99 rad/s=2π3.5 rad/s.

- *How to set the parameter* λ ?

The choice of the λ value must take into account the following points: 1) for lower λ values (close to zero), when the dc-link voltage error $|\Delta V_{dc}|$ increases, the selected ω_n value increases faster and shorter transient time can be achieved; 2) for higher λ values (close to 1), smoother ω_n selected value is obtained during steady state operation. In this paper, the λ value was set to 1 in order to select ω_n value approximately equal to $\omega_{n\min}$ during steady state operation to reduce grid current THD.

B. Simulation results

Simulations are done in order to compare the performances of the adaptive PI controller (including the anti-wind-up action) with those of the standard PI controller. The used simulation parameters are depicted on Tab.1 and the obtained simulation results are shown on Fig.3. Fig.3.a compares between simulations results obtained with the standard PI control (for constant PI gains tuned for $\omega_n=\omega_{n\min}$ and $\omega_n=\omega_{nopt}$) and those obtained with the proposed adaptive PI control. The natural frequency ω_{nopt} is determined so that, when a step jump equal to $I_{\max}$ is applied to the input current i, the resulting M_p value is equal to $G_{dc}V_{dc}^*=10\%V_{dc}^*$. So, based on equation (9), ω_{nopt} is computed as follows

$$\omega_{nopt}=F_5(0.7)\frac{I_{\max}}{G_{dc}V_{dc}^*}=\frac{416.88\times 1.25}{0.1*150}=34.74\text{rad/s} \quad (16)$$

It can be noted that the adaptive PI control ensures shorter transient time with lower drop of the dc-link voltage after a step jump (at t=0.5s) of the input current i equal to $I_{\max}$.

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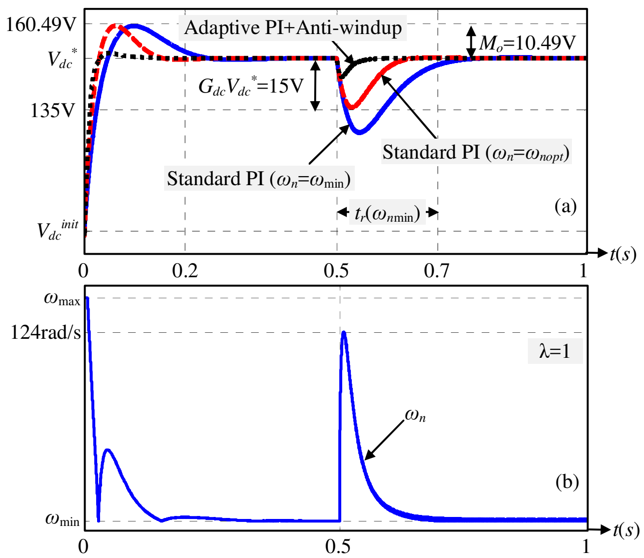

Fig. 3. Simulation results (ξ=0.7, V_{dc}^{init}=100V, V_{dc}^*=150, i=0 at t=0s and i=I_{max} at t=0.5s) (a) Comparison between standard PI control and adaptive PI control (b) waveform of the selected ω_n value for the adaptive PI controller

TABLE I
SYSTEM PARAMETERS

Symbol	Description	value	unit
S	GcC rated power	20	kVA
L	Inductive filter	40	mH
C	Dc-link voltage capacitor	1100	µF
Z_{load}	Load Impedance	120	Ω
I_{max}	Maximum load current	1.25	A
V_{dc_init}	DC-link voltage initial value	100	V
V_{dc}^*	Dc-link voltage reference value	150	V
G_{dc}	Ratio of the DC-link voltage band	10	%
λ	Used coefficient for ω_n computation	1	-
ω_{nmax}	Maximal natural frequency	2π22.73	rad/s
ω_{nopt}	Optimal natural frequency	2π5.35	rad/s
ω_{nmin}	Minimal natural frequency	2π3.5	rad/s
ξ	Damping ratio	0.7	-
K_c	Anti-windup coefficient	0.02	-
T_s	Sampling period	50	µs

Fig.3.b illustrates the waveform of the selected ω_n value for the adaptive PI controller. Notice that ω_n is almost equal to ω_{nmin} during steady state operation. During transient states it increases considerably and becomes equal to ω_{nmax} when the magnitude of the dc-link voltage error exceeds the band limit (during startup). It should be noted here that the maximum overshoot resulting from a step jump of the input current i equal to I_{max} at t=0.5s is significantly lower for the case of an adaptive PI controller compared to the case of a standard PI controller with constant gains and tuned for ω_n=ω_{nopt}. Moreover, as the selected ω_n value used for updating the ($\check{K}_{pdc}$, $\check{K}_{pdc}$) gains of the adaptive PI controller increases rapidly when the magnitude of the dc-link voltage error increases, the obtained M_p value with the adaptive PI controller can be approximated to that obtained for a standard PI controller with constant gains tuned for ω_n=ω_{nmax}.

IV. Experimental Results

In order to verify the efficiency of the proposed controller, the prototyping platform presented on Fig. 4 was developed. It includes three parts. The first one is a power part, which is composed of: 1) a three-phase autotransformer used to impose the desired grid voltage peak magnitude; 2) a three-phase inductive filter L; 3) a three-phase GcC; 4) a DC-link capacitor C; and 5) a resistive load Z_{Load}. The second one is the control part composed of 1) the STM32F4-Discovery digital solution and 2) a Host PC. Note that the used digital solution is based on Cortex-M4-ARM processor, which is associated to a Floating Point Unit (FPU) and have a system clock frequency equal to 168 MHz. Finally, the third part is an interface part that includes:1) a measurement board used to acquire seven analog measurements ($V_{g(a,b,c)}$, $i_{g(a,b,c)}$ and V_{dc}) and 2) an interface board used to amplify the computed switching signals $S_{(a,b,c)}$. The used parameters for the experimental tests are the same as the ones presented in Tab.1.

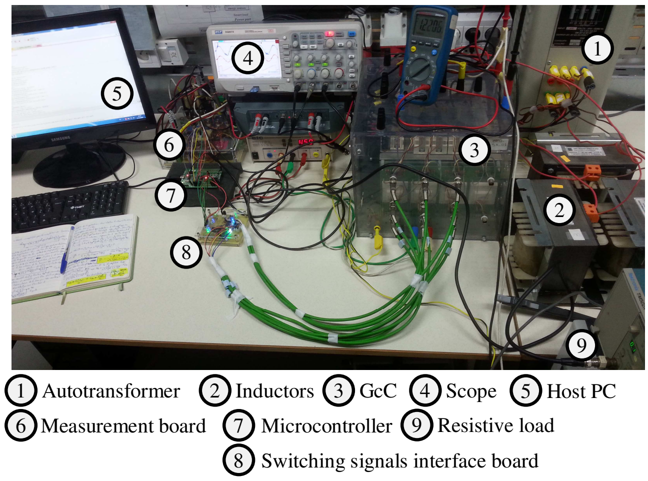

Fig. 4. Experimental set-up

In order to eliminate noises in the measured dc-link voltage, equation (15) was implemented with a small modification. The selected $\omega_n[k]$ value during a k^{th} sampling period is computed by replacing $|\Delta V_{dc}[k]|$ in (15) by $|\Delta V_{dc}|_{\min}[k]$, which is equal to the minimal value of $(|\Delta V_{dc}(j)|_{j=(k-n+1\ldots k)}$ (n was set to 5 for efficient elimination of the noises). The experimental tests were done according to the following steps:

- **Step 1**: The GcC switching signals were all tied at a low logical level. For that case, the GcC works as a simple three-phase diode bridge rectifier and the capacitor charge was initially set to 100V by acting on the ratio of the autotransformer. Also, the load Z_{load} was disconnected.

- **Step 2**: The switching signals $S_{(a,b,c)}$ were applied to the GcC and a step jump equal to 150V is applied to the dc-link voltage reference V_{dc}^*. The experimental results related to step 1 and 2 are presented in Fig.5.a, Fig.5.b and Fig.5.c. These figures compare between three cases: 1) a standard PI controller tuned for ω_n=ω_{nmin} (Fig.5.a), 2) a standard PI controller tuned for ω_n=ω_{nopt} (Fig.5.b) and 3) the proposed controller (Fig.5.c). It can be noted that the proposed controller ensures a dc-link voltage step response with good dynamic performances and without overshoot during the first transient states.

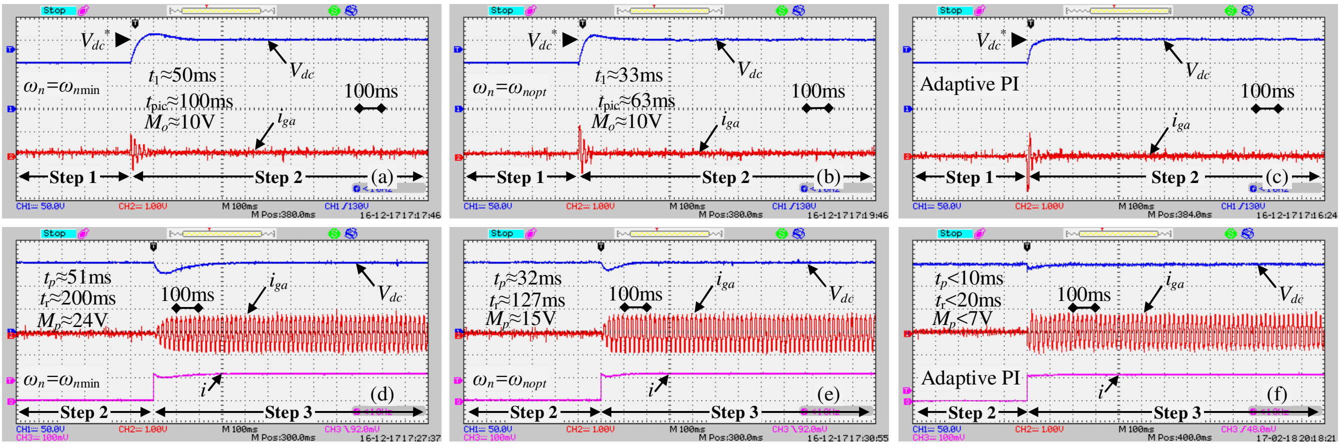

Fig. 5. (a-b-c) DC-link voltage V_{dc} (50V/div) and grid current i_{ga} (3.28A/div) waveforms during steps 1 and 2 (a) Standard PI controller (ω_n=ω_{nmin}) (b) Standard PI controller (ω_n=ω_{nopt}) (c) Proposed adaptive PI controller (e-f-g) DC-link voltage V_{dc} (50V/div) and grid current i_{ga} (3.28A/div) waveforms during steps 2 and 3 (e) Standard PI controller (ω_n=ω_{nmin}) (f) Standard PI controller (ω_n=ω_{nopt}) (g) Proposed adaptive PI controller

- Step 3: As explained previously, the proposed method supposes that the input current will not exceed a predefined maximum value $I_{\max}$. The worst case that will lead to a maximum overshoot value M_p is a sudden and sever change of the input current i that can be approximated to a step jump from 0 to $I_{\max}$ (for a sudden maximum power load connection). For others kinds of loads, characterized by a smoother input current i change, the overshoot will be lower than the considered worst case. During step 3, the control performances in terms of disturbance rejection were tested through a sudden connection of a resistive load Z_{Load} equal to V_{dc}^*/I_{max}=150V/1.25A=120Ω. The experimental results related to steps 2 and 3 are presented in Fig.5.d, Fig.5.e and Fig.5.f. These figures compare between three cases: 1) a standard PI controller tuned for ω_n=ω_{nmin} (Fig.5.d), 2) a standard PI controller tuned for ω_n=ω_{nopt} (Fig.5.e) and 3) the proposed controller (Fig.5.f). It can be noticed that the input current i response can be approximated to a step jump from 0 to I_{max} and that the obtained experimental results are quite close to those obtained in simulation results shown in Fig.3.

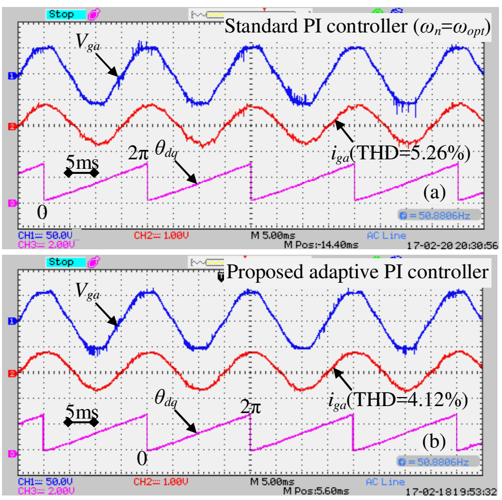

Fig. 6. Grid voltage V_{ga} (50V/div), grid current i_{ga} (3.28A/div) and grid voltage position θ_{dq} waveforms during steady state operation and using (a) a standard PI controller tuned for ω_n=ω_{nopt} (b) the adaptive PI controller

Finally, Fig.6 shows the grid voltage V_{ga} waveform with regard to the grid current i_{ga} and the estimated θ_{dq} position waveforms during steady state operation for a standard PI controller tuned for ω_n=ω_{nopt} (Fig.6.a) and for the proposed adaptive PI controller (Fig.6.b). This figure shows that a unitary power factor operation was achieved for both cases. Also, the use of the adaptive PI controller allowed the reduction of the grid current THD (the THD was reduced from 5.26% for the case of a standard PI controller to 4.12% for the proposed controller).

V. Conclusion

This paper presented an improved dc-link voltage controller based on an adaptive PI controller with an anti-windup process. The proportional and integral gains of the proposed PI controller are self-tuned so that the following constraints are satisfied: 1) no overshoot after step jumps of the dc-link voltage reference input; 2) fast dynamic response after step jumps of the dc-link voltage reference; 3) fast dynamic response after step jump of the input current i and 4) low grid current THD value during steady state operation. The considered control was experimentally tested on a prototyping platform. The obtained experimental results are quite similar to simulation results and show the effectiveness and reliability of the adopted control strategy.

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