Optimization Assessment of a New Extended Multilevel Converter Topology

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***Abstract*—In this paper, a novel general circuit for multilevel converter is presented. To produce all voltage levels, two methods are provided for selecting the amplitudes of sources. The proposed cascade structure is optimized for producing maximum levels with the least number of IGBTs, drivers, and dc sources. The proposed circuit is compared with other recommended multilevel converters. The comparison results prove the merits of proposed structure in terms of utilizing the least number of IGBTs and gate drivers. Also, the value of blocking voltage of all switches in the presented topology is low. The performance of the presented multilevel converter is indicated through simulated and experimented circuits.**

***Index Terms*—Blocking voltage of switches, multilevel converter, optimized topology, submultilevel.**

I. Introduction

RECENTLY, multilevel converters have been used in several industrial activities such as renewable energies, motor drives, FACTS devices, and so on [1]–[3]. Multilevel converters have numerous benefits over a traditional two-level converter such as improved output voltage quality or reduction of THD and the stress on switching devices [4]. Classical multilevel converters like diode-clamped converter [5] suggested by Nabae and flying-capacitor converter recommended by Meynard and Foch [6] have many disadvantages, if the number of levels goes up. Factually, the number of used semiconductors, clamping diodes, and capacitors increases substantially. To produce higher levels, cascade H-bridge (CHB) converter was used instead of other mentioned converters. This is due to the use of fewer numbers of switches. However, this structure needs isolated dc voltage sources. Several methods have been recommended for determination of the values of dc sources in CHB converter. The most popular methods were called binary and trinary methods [7], [8]. In [9], a new multilevel converter has been recommended which comprises of cascaded connection of submultilevel units. One clear restriction of this topology is the utilizing many switches.

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Other new cascade multilevel converter structures have been recommended in [10]–[16]. Each one of these structures has some disadvantages and advantages in terms of the number of components and voltage on switches. The presented topologies in [10] and [15] use a full-bridge converter in their structures. It causes the switches of full-bridge withstand high-voltage level. Then, these topologies are suitable for low-voltage applications. However, CHB and presented topologies in [9], [11], [12], and [14] utilize several full-bridges, which cause the blocking voltage on the switches to be reduced.

The presented topologies in [9]–[12], and [14] comprises series connection of extended submultilevel converters. Then, these topologies can be designed by various numbers of IGBTs, drivers, and sources in each submultilevel. Hence, to reduce the size and cost of these topologies, optimization of these topologies have been analyzed for generating maximum levels with minimum number of components. In addition to the proposed topologies in [10]–[16], modular multilevel converter (MMC) is an attractive topology for high-voltage applications such as high-voltage direct current systems. MMC topology consists of series connection of several submodules. The modularity of MMC topology is simple and its efficiency is high. However, the size and cost of MMC topology is high in comparison with the proposed topologies in [10]–[16] due to the using higher numbers of devices [17]. Also, balancing the capacitor voltages of submodules at their nominal values is another problem which needs active voltage-balancing techniques [18].

Matrix multilevel converter is another type of multilevel converter topology which is mostly used as a three-phase to three-phase ac–ac converter. This topology can increase and decrease the voltage magnitude and frequency. Moreover, it can operate with various power factors. However, multilevel converters and MMC cannot regulate the magnitudes of voltage, frequency, and power factor [19], [20].

II. Proposed Cascade Multilevel Converter Structure

To investigate the performance of the proposed cascade topology, the structure of the introduced basic unit is discussed, first. Then, the operation of proposed submultilevel converter is described. Finally, the structure of proposed cascade topology is investigated.

A. Proposed Basic Unit

The circuit of presented basic unit is illustrated in Fig. 1. This topology consists of two bidirectional switches

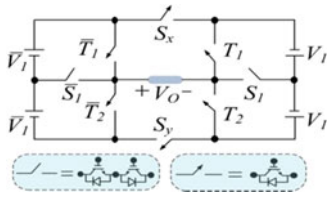

Fig. 1. Structure of the presented basic unit.

TABLE I
SWITCHING STATES OF PROPOSED BASIC UNIT

State	*ON Switches*	V_O
1	$\bar{T}_1, S_x, T_1$ $\bar{T}_2, S_y, T_2$	0
2	$\bar{S}_1, T_2, S_y$	$\bar{V}_1$
3	$\bar{S}_1, T_1, S_x$	$-\bar{V}_1$
4	$S_1, \bar{T}_2, S_y$	V_1
5	$S_1, \bar{T}_1, S_x$	$-V_1$
6	$\bar{T}_1, T_2, S_y$	$2\bar{V}_1$
7	$T_1, \bar{T}_2, S_x$	$-2\bar{V}_1$
8	$T_1, \bar{T}_2, S_y$	$2V_1$
9	$\bar{T}_1, T_2, S_x$	$-2V_1$
10	$S_1, \bar{S}_1, S_y$	$\bar{V}_1 + V_1$
11	$S_1, \bar{S}_1, S_x$	$-(\bar{V}_1 + V_1)$
12	$\bar{T}_1, S_1, S_y$	$2\bar{V}_1 + V_1$
13	$\bar{T}_2, S_1, S_x$	$-(2\bar{V}_1 + V_1)$
14	$\bar{S}_1, T_1, S_y$	$\bar{V}_1 + 2V_1$
15	$(\bar{V}_1, T_2, S_x$	$-(\bar{V}_1 + 2V_1)$
16	$T_1, \bar{T}_1, S_y$	$2\bar{V}_1 + 2V_1$
17	$T_2, \bar{T}_2, S_x$	$-(2\bar{V}_1 + 2V_1)$

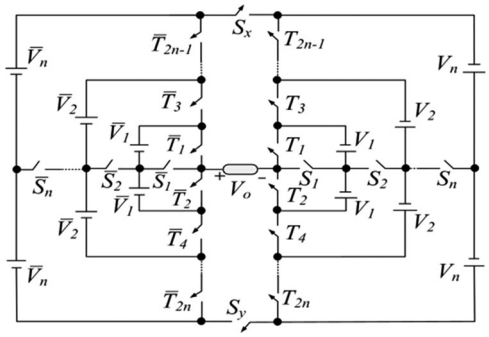

Fig. 2. Proposed submultilevel converter.

$(S_1, \bar{S}_1)$, four dc sources, and six unidirectional switches $(T_1, T_2, \bar{T}_1, \bar{T}_2, S_x, S_y)$. Each unidirectional switch comprises of an antiparallel diode and an IGBT. The type of bidirectional switches is common-emitter that consists of two IGBTs and two antiparallel diodes and requires only one gate driver. Two of dc sources have the same amplitude of $\bar{V}_1$ and the value of other two sources is V_1. Table I indicates the switching states of proposed basic unit to produce all levels at output voltage.

B. Proposed Submultilevel Converter

The basic unit can be extended to increase the number of levels, which is indicated in Fig. 2. This topology is named submultilevel converter and consists of several legs. Each leg has two sources with the same magnitudes. However, the values of sources in each leg differ from other legs. Table II shows the switching pattern of the proposed submultilevel topology. It is notable that the proposed submultilevel topology consists of a back-to-back double-side T-shape multilevel converter along with an extended H-bridge.

TABLE II
SWITCHING STATES OF PROPOSED SUBMULTILEVEL CONVERTER

ON Switches	V_O
$\bar{T}_1, \bar{T}_3, \ldots, \bar{T}_{2n-1}, T_1, T_3, \ldots, T_{2n-1}, S_y$	$2V_{n-1} + 2V_n$
$\bar{S}_1, \bar{T}_3, \ldots, \bar{T}_{2n-1}, T_1, T_3, \ldots, T_{2n-1}, S_y$	$2V_3 + 2V_4 - V_1$
⋮	⋮
$\bar{S}_1, \bar{T}_4, \ldots, \bar{T}_{2n}, T_2, T_4, \ldots, T_{2n}, S_y$	V_1
$\bar{T}_1, \bar{T}_3, \ldots, \bar{T}_{2n-1}, T_1, T_3, \ldots, T_{2n-1}, S_x$	0
$\bar{S}_1, \bar{T}_3, \ldots, \bar{T}_{2n-1}, T_1, T_3, \ldots, T_{2n-1}, S_x$	$-V_1$
⋮	⋮
$\bar{S}_1, \bar{T}_4, \ldots, \bar{T}_{2n}, T_2, T_4, \ldots, T_{2n}, S_x$	$-(2V_3 + 2V_4 - V_1)$
$\bar{T}_2, \bar{T}_4, \ldots, \bar{T}_{2n}, T_2, T_4, \ldots, T_{2n}, S_x$	$-(2V_3 + 2V_4)$

C. Proposed Cascade Multilevel Converter Structure.

To increase the number of levels, a cascade multilevel converter based on a series connection of z submultilevel converters is proposed, which is indicated in Fig. 3. The output voltage of the proposed cascade converter (V_{out}) is the sum of output voltages of submultilevel converters. In other words,

$$\mathrm{V}_{\text{out}} = \mathrm{V}_{\text{o},1} + \mathrm{V}_{\text{o},2} + \cdots + \mathrm{V}_{\text{o,z}}. \tag{1}$$

The structure of the first, second, ..., and zth submultilevel converter comprises of $2n_1$, $2n_2$, ... and $2n_z$ bidirectional switches, respectively. To produce maximum levels with constant number of devices, we have to consider that the number of bidirectional switches in each submultilevel is the same. In other words,

$$n_1 = n_2 = \ldots = n_z = n. \tag{2}$$

Considering (2), the number of IGBTs (N_{IGBT}) used, drivers (N_{driver}), and dc sources (N_{dc}) in the recommended cascade topology are obtained by (3)–(5), respectively,

$$N_{\text{IGBT}} = z(8n + 2) \tag{3}$$

$$N_{\text{driver}} = z(6n + 2) \tag{4}$$

$$N_{\text{dc}} = 4nz. \tag{5}$$

III. Determination of the Values of DC Sources

Based on Fig. 3, each submultilevel converter consists of several legs. As indicated in this figure, the values of dc sources in each leg are equal. However, the values of dc sources in independent legs are nonequal. To produce all levels at output voltage, two methods are recommended for dc sources values of proposed converter as follows:

A. First Method

In the first method, the values of sources in each sum-multilevel are determined using the following relationships.

First submultilevel.

$$\bar{V}_{1j} = 5^{j-1} V_{\text{dc}}, \qquad \text{for } j = 1, 2, \ldots, n \tag{6}$$

$$V_{1j} = 2 \times 5^{j-1} V_{\text{dc}}, \qquad \text{for } j = 1, 2, \ldots, n. \tag{7}$$

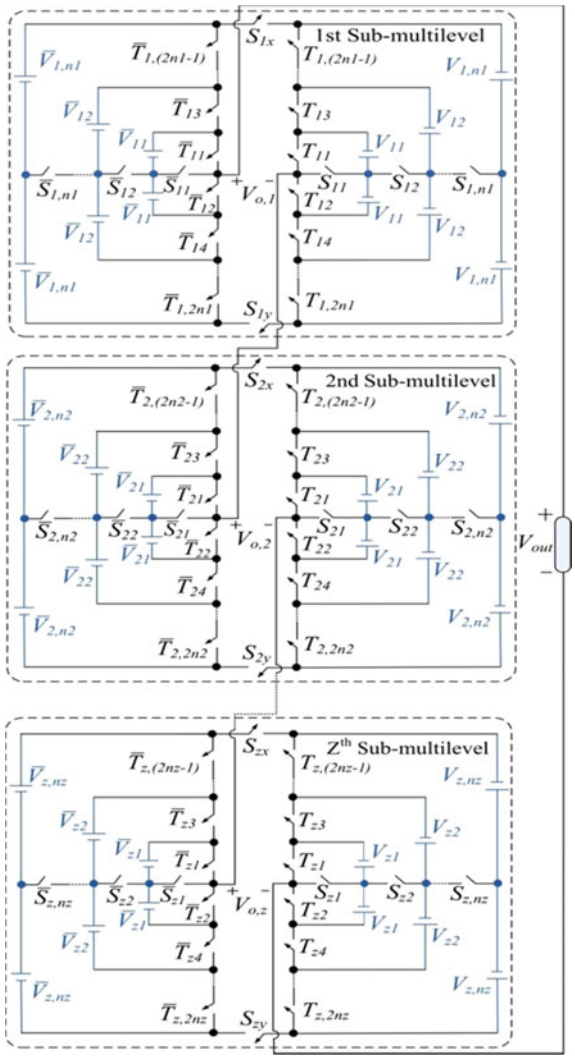

Fig. 3. Proposed cascade multilevel converter topology.

In this submultilevel, the maximum magnitude of output voltage $(V_{o,1,\max})$ will be

$$V_{o,1,\max} = 2(\bar{V}_{1,n1} + V_{1,n1}) = 6 \times 5^{n-1} V_{\rm dc}. \quad (8)$$

Second submultilevel:

$$\bar{V}_{2j} = 5^{j-1}(V_{\rm dc} + V_{o,1,\max})$$
$$= 5^{j-1}(1 + 6 \times 5^{n-1})V_{\rm dc}, \quad \text{for } j = 1, \ldots, n \quad (9)$$
$$V_{2j} = 2 \times 5^{j-1}(1 + 6 \times 5^{n-1})V_{\rm dc}, \quad \text{for } j = 1, \ldots, n. \quad (10)$$

In this submultilevel, the value of maximum output voltage $(V_{o,2,\max})$ will be

$$V_{o,2,\max} = 2(\bar{V}_{2,n2} + V_{2,n2}) = 6 \times 5^{n-1}(V_{\rm dc} + 6 \times 5^{n-1} V_{\rm dc}). \quad (11)$$

*z*th *submultilevel*:

$$\bar{V}_{zj} = 5^{j-1}\left(V_{\rm dc} + \sum_{i=1}^{z-1} V_{o,i,\max}\right)$$
$$\bar{V}_{zj} = 5^{j-1}(1 + 6 \times 5^{n-1})^{z-1} V_{\rm dc} \quad \text{For } j = 1, \ldots, n \quad (12)$$
$$V_{zj} = 2 \times 5^{j-1}(1 + 6 \times 5^{n-1})^{z-1} V_{\rm dc} \quad \text{For } j = 1, \ldots, n. \quad (13)$$

According to this method, the number of generated levels in the present first method $(N_{\text{level},F})$ will be

$$N_{\text{level},F} = (12 \times 5^{n-1} + 1)^z. \quad (14)$$

B. Second Method

According to this method, dc sources magnitudes in each submultilevel are selected considering the following algorithms:

First submultilevel:

$$\bar{V}_{1j} = 10^{j-1} V_{\rm dc}, \quad \text{for } j = 1, 2, \ldots, n \quad (15)$$
$$V_{1j} = 3 \times 10^{j-1} V_{\rm dc}, \quad \text{for } j = 1, 2, \ldots, n. \quad (16)$$

Based on (15), (16), $V_{o,1,\max}$ is

$$V_{o,1,\max} = 2(\bar{V}_{1,n1} + V_{1,n1}) = 8 \times 10^{n-1} V_{\rm dc}. \quad (17)$$

Second submultilevel:

$$\bar{V}_{2j} = 10^{j-1}(V_{\rm dc} + V_{o,1,\max})$$
$$= 10^{j-1}(1 + 8 \times 5^{n-1})V_{\rm dc}, \quad \text{for } j = 1, \ldots, n \quad (18)$$
$$V_{2j} = 3 \times 10^{j-1}(1 + 8 \times 10^{n-1})V_{\rm dc}, \quad \text{for } j = 1, \ldots, n. \quad (19)$$

The value of $V_{o,2,\max}$ is:

$$V_{o,2,\max} = 2(\bar{V}_{2,n2} + V_{2,n2}) = 8 \times 10^{n-1}(1 + 8 \times 10^{n-1})V_{\rm dc}. \quad (20)$$

*z*th *submultilevel*:

$$\bar{V}_{z,jz} = 10^{j-1}(V_{\rm dc} + \sum_{i=1}^{z-1} V_{o,i,\max})$$
$$= 10^{j-1}(1 + 8 \times 10^{n-1})^{z-1} V_{\rm dc}, \quad \text{for } j = 1, \ldots, n \quad (21)$$
$$V_{z,jz} = 3 \times 10^{j-1}(1 + 8 \times 10^{n-1})^{z-1} V_{\rm dc}, \quad \text{for } i = 1, \ldots, n. \quad (22)$$

The number of generated levels in the proposed second method $(N_{\text{level},S})$ is

$$N_{\text{level},S} = (16 \times 10^{n-1} + 1)^z. \quad (23)$$

IV. Calculation of Blocking Voltage on Switches

The blocking voltage of all switches (V_{sw}) is an important parameter in multilevel converters because its reduction leads to the reduction of costs. To calculate this parameter, we have

$$V_{\rm sw} = V_{{\rm sw},u} + V_{{\rm sw},b}. \quad (24)$$

In this equation, $V_{{\rm sw},u}$ and $V_{{\rm sw},b}$ are the magnitudes of blocking voltage of unidirectional and bidirectional switches, respectively. $V_{{\rm sw},b}$ is obtained as follows:

$$V_{{\rm sw},b} = \sum_{j=1}^{n} \sum_{i=1}^{z} (V_{\bar{S}_{ij}} + V_{S_{ij}}). \quad (25)$$

To calculate $V_{{\rm sw},b}$, the blocking voltage of bidirectional switches in the *i*th submultilevel converter (i = 1, 2, ..., z)

are calculated. Then, the obtained results can be extended for other submultilevel converters. In other words,

$$V_{\bar{S}_{i1}} = \bar{V}_{i1} \tag{26}$$

$$V_{S_{i1}} = V_{i1} \tag{27}$$

$$V_{\bar{S}_{i2}} = \bar{V}_{i2} - \bar{V}_{i1} \tag{28}$$

$$V_{S_{i2}} = V_{i2} - V_{i1} \tag{29}$$

$$V_{\bar{S}_{i,ni}} = \bar{V}_{i,ni} - \bar{V}_{i,(n-1)i} \tag{30}$$

$$V_{S_{i,ni}} = V_{i,ni} - V_{i,(n-1)i} \tag{31}$$

where $V_{\bar{S}_{i1}}, V_{S_{i1}}, V_{\bar{S}_{i2}}, V_{S_{i2}}, ..., V_{\bar{S}_{i,ni}}, V_{S_{i,ni}}$ are the values of blocking voltage on the switches of $\bar{S}_{i1}, S_{i1}, \bar{S}_{i2}, S_{i2}, ..., \bar{S}_{i,ni}, S_{i,ni}$ in the *i*th submultilevel converter, respectively. Therefore, substituting (26)–(31) in (25), the blocking voltage on all bidirectional switches in proposed cascade topology is

$$V_{\mathrm{sw},b} = \sum_{i=1}^{z} (V_{i,ni} + \bar{V}_{i,ni}). \tag{32}$$

To compute $V_{sw,u}$, we have

$$V_{\mathrm{sw},u} = \sum_{j=1}^{2n} \sum_{i=1}^{z} (V_{\bar{T}_{ij}} + V_{T_{ij}} + V_{S_{ix}} + V_{S_{iy}}) \tag{33}$$

where $V_{\bar{T}_{ij}}, V_{T_{ij}}, V_{S_{ix}}$, and $V_{S_{iy}}$ are the value of blocked voltage on the switches $\bar{T}_{ij}, T_{ij}, S_{ix}$ and S_{iy} in the *j*th unidirectional switch of the *i*th submultilevel converter. To simplify and obtain this equation, we calculate the blocked voltage on the unidirectional switches of the *i*th submultilevel converter ($i = 1, 2, \ldots, z$). Then, the results can be extended for other submultilevel converters. In other words,

$$V_{\bar{T}_{i1}} = V_{\bar{T}_{i2}} = 2\bar{V}_{i1} \tag{34}$$

$$V_{\bar{T}_{i3}} = V_{\bar{T}_{i4}} = 2\bar{V}_{i2} - 2\bar{V}_{i1} \tag{35}$$

$$V_{\bar{T}_{i,(2n-1)i}} = V_{\bar{T}_{i,2ni}} = 2\bar{V}_{i,ni} - 2\bar{V}_{i,(n-1)i} \tag{36}$$

$$V_{T_{i1}} = V_{T_{i2}} = 2V_{i1} \tag{37}$$

$$V_{T_{i3}} = V_{T_{i4}} = 2V_{i2} - 2V_{i1} \tag{38}$$

$$V_{T_{i,(2n-1)i}} = V_{T_{i,2ni}} = 2V_{i,ni} - 2V_{i,(n-1)i} \tag{39}$$

$$V_{S_{ix}} = V_{S_{iy}} = 2\bar{V}_{i,ni} + 2V_{i,ni} \tag{40}$$

where $V_{\bar{T}_{i1}}, V_{\bar{T}_{i2}}, V_{T_{i1}}, V_{T_{i2}}, ..., V_{\bar{S}_{i,2ni}}, V_{S_{i,2ni}}, V_{S_{ix}}, V_{S_{iy}}$ are the values of blocked voltage on the $\bar{T}_{i1}, \bar{T}_{i2}, T_{i1}, T_{i2}, ..., \bar{S}_{i,2ni}, S_{i,2ni}, S_{ix}, S_{iy}$ in the *i*th submultilevel converter, respectively. The mentioned equations in (34)–(40) can be applied for all submultilevel converters such as the first, second, ..., and *z*th submultilevel converter (or $i = 1, 2, \ldots, z$). Then, considering (33) and (34)–(40), the value of blocked voltage by unidirectional switches can be simplified as follows:

$$V_{\mathrm{sw},u} = 8 \sum_{i=1}^{z} (V_{i,ni} + \bar{V}_{i,ni}). \tag{41}$$

Therefore, substituting (32) and (41) in (24), the value of total blocked voltage by all switches is obtained as follows:

$$V_{\mathrm{sw}} = 9 \sum_{i=1}^{z} (V_{i,ni} + \bar{V}_{i,ni}). \tag{42}$$

The maximum output voltage of proposed topology is

$$V_{\mathrm{out,max}} = 2 \sum_{i=1}^{z} (\bar{V}_{i,ni} + V_{i,ni}). \tag{43}$$

Using (42) and (43), it is clear that

$$V_{\mathrm{sw}} = \frac{9V_{\mathrm{out,max}}}{2}. \tag{44}$$

The value of $V_{\mathrm{out,max}}$ can be recalculated as follows:

$$V_{\mathrm{out,\,max}} = \left(\frac{N_{\mathrm{level}} - 1}{2}\right) V_{\mathrm{dc}}. \tag{45}$$

By the combination of (44) and (45), the value of V_{sw} will be

$$V_{\mathrm{sw}} = \frac{9(N_{\mathrm{level}} - 1)}{4} V_{\mathrm{dc}}. \tag{46}$$

Current rating of the switches is another important parameter which effects on the cost of converter. However, the maximum current of the switches in the recommended circuit and other recommended topologies in [10]–[16] is equal to the maximum current of the load, when the switch is in the ON-state. It is clear that when the switch is in the OFF-state, the current is zero. Therefore, the current of switches in the recommended circuit is varied between zero and maximum current of the load. However, the current stress of switches (or I_{rms}) is related to different parameters such as modulation index, switching angles, and the number of generated levels at output voltage waveforms and is calculated as follows:

$$I_{\mathrm{rms}} = \sqrt{\frac{1}{2\pi} \int_0^{\pi} {i_{\mathrm{sw}}}^2 dwt} \tag{47}$$

where i_{sw} is the current passing through switch.

V. Optimization of the Proposed Cascade Topology

The main aim of optimization of proposed cascade topology is that what number of switches, drivers, and dc sources must be used in each submultilevel to attain maximum levels.

A. Optimized Cascade Converter to Produce Maximum Levels With Constant N_{IGBT}

Generating maximum N_{level} with constant N_{IGBT} is the main goal of this section. Considering (3), we have

$$z = \frac{N_{\mathrm{IGBT}}}{8n + 2}. \tag{48}$$

Substituting (48) in (14) and (23), the number of generated levels based on the presented methods is

$$N_{\mathrm{level},F} = \left[(12 \times 5^{n-1} + 1)^{1/8n+2}\right]^{N_{\mathrm{IGBT}}} \tag{49}$$

$$N_{\mathrm{level},S} = \left[(16 \times 10^{n-1} + 1)^{1/8n+2}\right]^{N_{\mathrm{IGBT}}}. \tag{50}$$

Variation of $(12 \times 5^{n-1} + 1)^{1/8n+2}$ and $(16 \times 10^{n-1} + 1)^{1/8n+2}$ against *n* is indicated in Fig. 4(a). It is obvious that the maximum number of levels for the first proposed method can be obtained for $n = 1$. Also, the maximum number of levels according to the recommended second method is obtained for $n = \infty$. It means that the proposed topology consists of only one

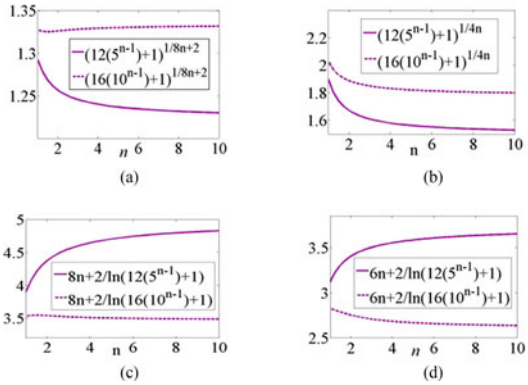

Fig. 4. Related curves to the optimization analysis to obtain n considering (a) maximum N_{level} with constant N_{IGBT}, (b) maximum N_{level} with constant N_{dc}, (c) minimum N_{IGBT} with constant N_{level}, and (d) minimum N_{driver} with constant N_{level}.

extended submultilevel ($z = 1$) to attain maximum levels (see Fig. 2).

B. Optimized Cascade Converter for Maximum N_{level} With Constant N_{dc}

The main goal of this section is determining the value of n to produce maximum N_{level} with constant N_{dc}. Considering (4), it is obvious that

$$z = \frac{N_{\text{dc}}}{4n}. \tag{51}$$

Replacing (51) in (14) and (23), $N_{\text{level},F}$ and $N_{\text{level},S}$ can be obtained by (52) and (53), respectively,

$$N_{\text{level},F} = \left[(12 \times 5^{n-1} + 1)^{1/4n}\right]^{N_{\text{dc}}} \tag{52}$$

$$N_{\text{level},S} = \left[(16 \times 10^{n-1} + 1)^{1/4n}\right]^{N_{\text{dc}}}. \tag{53}$$

Variation of $(12 \times 5^{n-1} + 1)^{1/4n}$ and $(16 \times 10^{n-1} + 1)^{1/4n}$ versus n is illustrated in Fig. 4(b). It is obvious that $n = 1$ gives the optimal structure for both proposed methods.

C. Optimized Cascade Converter to Utilize Minimum N_{IGBT} With Constant N_{level}

Using (3), (14), and (23), N_{IGBTs} based on the proposed first and second methods are calculated as follows:

$$N_{\text{IGBT}} = \ln(N_{\text{level},F}) \times \frac{(8n+2)}{\ln(12 \times 5^{n-1} + 1)} \tag{54}$$

$$N_{\text{IGBT}} = \ln(N_{\text{level},S}) \times \frac{(8n+2)}{\ln(16 \times 10^{n-1} + 1)}. \tag{55}$$

In these equations, $N_{\text{level},F}$ and $N_{\text{level},S}$ are constant. Therefore, N_{IGBT} is minimized when $(8n+2)/\ln(12 \times 5^{n-1} + 1)$ and $(8n+2)/\ln(16 \times 10^{n-1} + 1)$ be minimum. Fig. 4(c) indicates that the least number of IGBTs based on the first method is given for $n = 1$. Moreover, the least number of used IGBTs based on the presented second method is obtained for $n = \infty$.

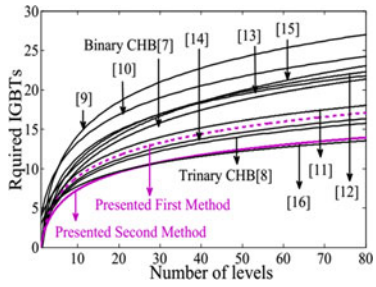

Fig. 5. Comparison of N_{IGBTs} in different structures.

D. Optimized Cascade Converter for Minimum N_{driver} With Constant N_{level}

Considering (4), (14), and (23), the number of drivers in the circuit of cascade circuit according to the proposed first and second methods is obtained by (56) and (57), respectively,

$$N_{\text{driver}} = \ln(N_{\text{level},F}) \times \frac{(6n+2)}{\ln(12 \times 5^{n-1} + 1)} \tag{56}$$

$$N_{\text{driver}} = \ln(N_{\text{level},S}) \times \frac{(6n+2)}{\ln(16 \times 10^{n-1} + 1)}. \tag{57}$$

Variations of $(6n+2)/\ln(12 \times 5^{n-1} + 1)$ and $(6n+2)/\ln(16 \times 10^{n-1} + 1)$ versus n is indicated in Fig. 4(d). According to this figure, the least number of drivers based on the proposed first and second methods are obtained for $n = 1$ and $n = \infty$, respectively.

VI. Comparison Studies

To verify the value of proposed cascade topology, comparison results are provided in this section in terms of the number of devices and blocking voltage on switches. The optimized topologies considering various aspects are compared with Binary [7] and trinary CHB [8] topologies and presented topologies in [10]–[16]. It is notable that several methods for selecting the values of dc sources in the proposed topologies in [11], [13], and [15] were presented. For comparison, the best algorithms which can produce maximum levels with the least number of devices and voltage on switches are selected.

Fig. 5 compares the number of power IGBTs against the number of levels for recommended structure and suggested structures in [11]–[16]. Based on this figure, it is clear that the proposed topology requires the least number of IGBTs than [7]–[16] for N_{level} less than 39. However, the suggested structures in [16] requires almost one more IGBT than the suggested structures for N_{level} higher than 39.

The number of drivers against levels in different structures is indicated in Fig. 6. This figure indicates that recommended structure based on second algorithm requires minimum number of drivers compared to other structures.

The variation of the total blocked voltage rating on switches versus N_{level} at the output for different structures is indicated in Fig. 7. This comparison indicates that the blocking voltage on switches in the recommended cascade topology and [14] are similar and it is lower than proposed topologies in [9]–[13], and [15]. However, binary and trinary CHB and presented topology in [16] have the least value of voltage rating on switches. But it is clear that binary and trinary topologies require many switching

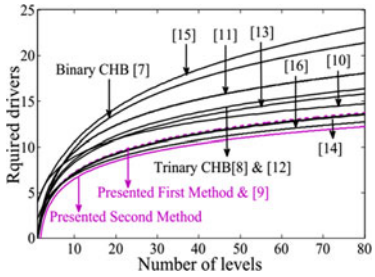

Fig. 6. Comparison of N_{driver} in different structures.

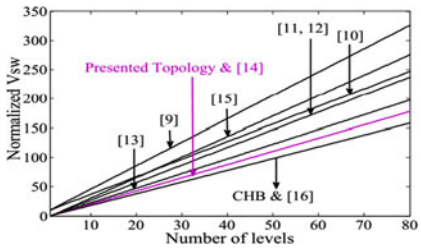

Fig. 7. Variation of blocking voltages on switches in different multilevel converter structures.

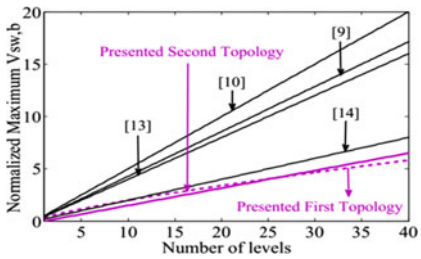

Fig. 8. Normalized maximum blocked voltages on bidirectional switch in different converters.

devices in comparison with the presented topology. The maximum blocking voltage on bidirectional switches in the proposed cascade converter is related to the switch $S_{n,zn}$, which have to withstand high voltage equal to $V_{z,nz} - V_{z,(n-1)z}$. The value of maximum voltage on bidirectional switch versus the number of levels in different topologies is shown in Fig. 8. This comparison indicates that the maximum voltage on bidirectional switch in the suggested cascade topology based on two proposed methods is less than other structures.

The switches S_x and S_y in the proposed submultilevel topology (see Fig. 2) withstand a voltage equal to maximum value of output voltage waveform. It causes the proposed submultilevel structure to be suitable for low-voltage applications. However, all switches in the proposed cascade topology (see Fig. 3) withstand a fraction of the amplitude of output voltage waveform. Then, the proposed cascade topology is a suitable candidate for high-voltage levels. It is notable that there are two unidirectional switches in the presented topology in [16], which tolerate maximum magnitude of output voltage. Also, there are four high-voltage unidirectional switches in the presented topologies in [10] and [15]. It causes the proposed topologies in [10], [15], and [16] to be suitable for low-voltage applications. The value of maximum blocked voltage rating on unidirectional switch versus N_{level} in different topologies is shown in Fig. 9. This

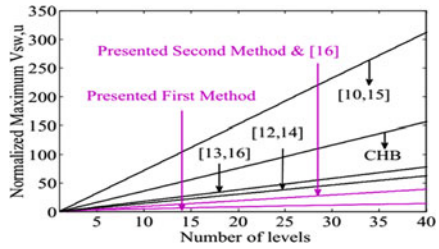

Fig. 9. Normalized maximum blocked voltages on unidirectional switch in different converters.

comparison indicates that the maximum voltage on unidirectional switch in the proposed topology based on the first method is less than other topologies.

Generally, using independent dc sources in the proposed topology and proposed topologies in [7]–[16] is not reasonable. To solve this problem, multitap transformer and one-input multioutput dc–dc converters are used. When an ac source is available, by the regulating the number of turns in the secondary sides of the multitapa transformer, the required multiple dc sources can be generated [21]. Also, when a dc source is available, using one-input multioutput dc–dc converters, the required multiple dc sources are created [22].

The proposed topology can be used in motor drives for harmonic elimination using selective harmonic elimination switching algorithms such as particle swarm optimization, Bee, and so on. Also, direct torque control is another application of presented topology in induction motor drives, which provides lower torque ripple. Moreover, the proposed topology is used in power system applications such as HVDC, reactive power compensation, compensation of voltage sag and swell caused by line fault, and so on.

VII. Power Losses Evaluation of Proposed Cascade Topology

There are two kinds of losses in switches which are called conduction and switching losses and are evaluated as follows:

A. Conduction Losses

The conduction losses (P_c) is obtained as follows:

$$P_c = V_{\mathrm{on}} \times I_l(t) \tag{58}$$

where V_{on} and I_l are the on-state voltage drop and the conducted current, respectively. It is assumed that the conducted current by switches is almost sinusoidal and it is calculated as follows:

$$I_l\,(t) = I_p \sin\,(wt)\,. \tag{59}$$

It is clear that the conduction losses include the conduction losses of an IGBT $(P_{c,\mathrm{IGBT}})$ and an antiparallel diode $(P_{c,D})$. $P_{c,\mathrm{IGBT}}$ and $P_{c,D}$ are evaluated as follows:

$$P_{c,\mathrm{IGBT}} = \left[V_{\mathrm{on,IGBT}} + R_{\mathrm{IGBT}}.{I_p}^{\alpha}(t)\right].I_p(t) \tag{60}$$

$$P_{c,D} = \left[V_{\mathrm{on},D} + R_D.I_p(t)\right].I_p(t). \tag{61}$$

In aforesaid equations, $V_{\mathrm{on},D}$ and $V_{\mathrm{on,IGBT}}$ are the drop voltage of on-state antiparallel diode and IGBT, respectively. Moreover, R_D and R_{IGBT} are the equivalent resistance of on-state antiparallel-diode and IGBT, respectively. α is a constant factor which is related to the specification of the IGBT. We suppose

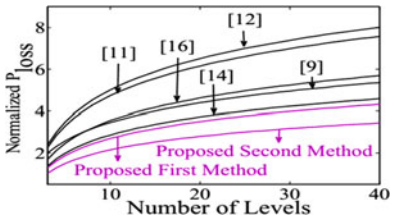

Fig. 10. Normalized maximum power losses in different converters.

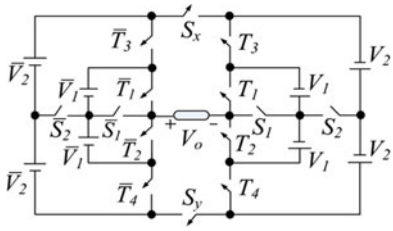

Fig. 11. Structure of 61-level submultilevel converter.

that there are $x(t)$ IGBTs and $y(t)$ antiparallel diodes in on-state in the current path at any time. Hence, the conduction losses of recommended converters (P_c) is

$$P_c = \frac{1}{2\pi}\int_0^{2\pi} [x(t)(P_{c,\mathrm{IGBT}}) + y(t)(P_{c,D})] \times I_p(t)d(wt). \tag{62}$$

B. Switching Losses

In order to evaluate switching losses, the linear variations of the current and voltage of the switch during turn-off and turn-on periods are considered. In the turn-off period of the switch, the dissipated energy (E_{off}) is

$$\begin{aligned} E_{\mathrm{off}} &= \int_0^{t_{\mathrm{off}}} V(t) \times I(t)dt \\ &= \int_0^{t_{\mathrm{off}}} -\frac{V_{IGBT} \times t}{t_{\mathrm{off}}} \times \frac{I(t - t_{\mathrm{off}})}{t_{\mathrm{off}}} d(t) \\ &= \frac{V_{\mathrm{IGBT}} \times I \times t_{\mathrm{off}}}{6} \end{aligned} \tag{63}$$

where V_{IGBT}, I, and t_{off} are the off-state voltage on the IGBT, the passing current through the IGBT before turning off, and the turn-off time of the IGBT, respectively. Moreover, the energy loss of the IGBT (E_{on}) is:

$$E_{\mathrm{on}} = \int_0^{t_{\mathrm{on}}} V(t) \times I(t)\mathrm{dt} = \int_0^{t_{\mathrm{on}}} -\frac{V_{\mathrm{IGBT}}.t}{t_{\mathrm{on}}} \times \frac{I(t - t_{\mathrm{on}})}{t_{\mathrm{on}}} \mathrm{d}(t)$$
$$= \frac{V_{\mathrm{IGBT}} \times I \times t_{\mathrm{on}}}{6} \tag{64}$$

where t_{on} is the on-state time of IGBT. The switching loss (P_{sw}) is equal to the sum of all turn-on and turn-off energy losses in a fundamental cycle of the output voltage, which is calculated as follows:

$$P_{\mathrm{sw}} = f \times [N_{\mathrm{off}} \times E_{\mathrm{off}} + N_{\mathrm{on}} \times E_{\mathrm{on}}]. \tag{65}$$

In this equation, f, N_{off}, and N_{on} are the fundamental frequency, the number of turning on and off IGBTs in a fundamental cycle, respectively. The normalized total power losses of various topologies are illustrated in Fig. 10. According to this figure, the normalized losses of proposed topology based on the two methods is less than the proposed topologies in [9], [11], [12], [14], and [16]. In this figure, we assume that the values of parameters for diodes and IGBTs are $R_T = 0.15\,\Omega$, $V_T = 2.5$ V, $R_D = 0.15\,\Omega$, $V_D = 1.5$ V. Moreover, the values of used R–L load are 45 Ω and 110 mH, respectively.

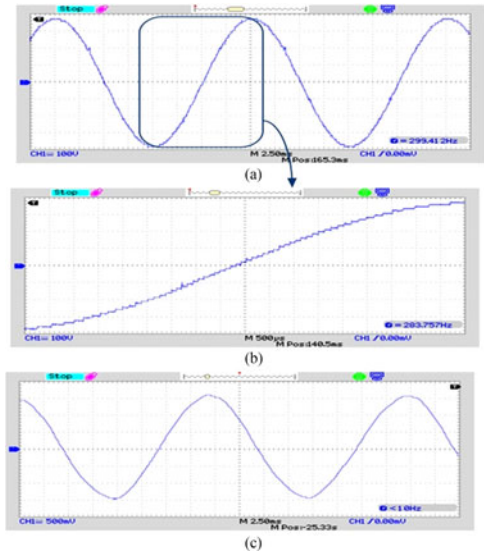

Fig. 12. Experimental waveforms of proposed 61-level converter, (a) complete waveform of output voltage, (b) half-cycle waveform of output voltage, and (c) output current.

VIII. Simulation and Experimental Results

To illustrate the operation of the recommended submultilevel converter and cascade structures, the experimental results for a 61-level based on the proposed sub-multilevel converter and simulation results for a 169-level cascade converter are presented. There are several switching patterns for multilevel topologies, where the most important methods are sinusoidal pulse width modulation (PWM) method, space vector PWM, fundamental frequency switching, etc. [23], [24]. Fundamental frequency switching is used to produce the pulses of switches. For simulation and experimental works, an R–L load with the values of $R = 270\ \Omega$ and $L = 60$ mH is used.

A. Experimental Results

Fig. 11 depicts the structure of 61-level submultilevel based on the first algorithm. The values of sources are

$$\bar{V}_1 = 13\ \mathrm{V},\ V_1 = 26\ \mathrm{V},\ \bar{V}_2 = 65\ \mathrm{V},\ V_2 = 130\ \mathrm{V}.$$

Fig. 12(a) shows the complete output voltage waveform of 61-level converter. Fig 12(b) illustrates the half-cycle waveform of output voltage, which the number of produced positive and negative levels can be counted clearly. The maximum output voltage is 390 V. Based on Fig. 10(b), the generated levels are 0, $\pm$13 V, $\pm$26 V, ..., $\pm$377 V, $\pm$390 V. Fig. 12(c) indicates the

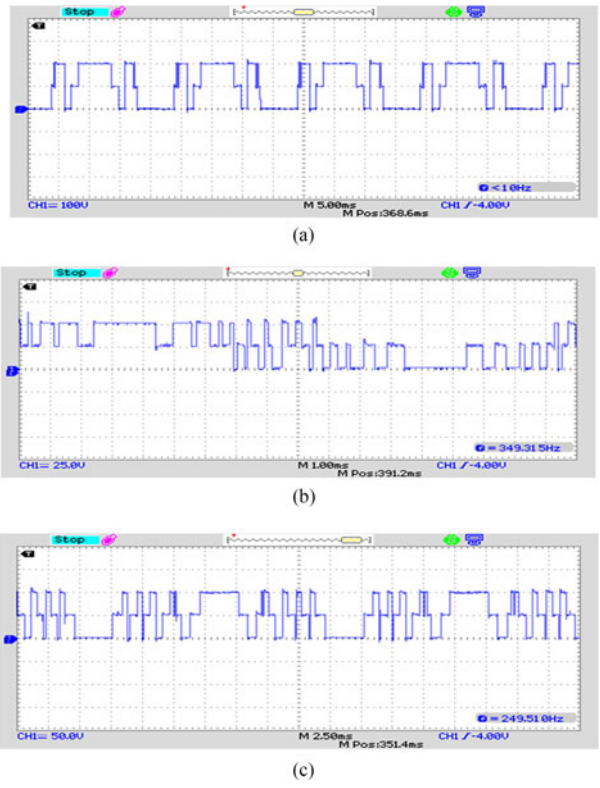

Fig. 13. Experimental voltage waveforms of some switches of 61-level converter (a) T_3, (b) T_1, and (c) $\bar{T}_3$.

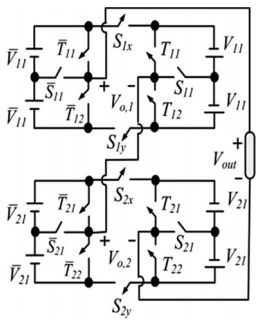

Fig. 14. 169-level converter based on the proposed cascade converter.

output current of the converter. Fig. 13(a)–(c) indicates the voltage waveform of the some unidirectional switches consisting of the switches T_3, T_1, and $\bar{T}_3$ where their maximum blocked voltage of these switches are 108, 52, and 104 V, respectively.

B. Simulation Results

For this section, PSCAD/EMTDC Simulink software has been used for simulation. Fig. 14 indicates the circuit of a 169-level cascade converter based on the proposed first method. In this topology, the values of dc sources based on the proposed first algorithm are selected as follows:

$$\bar{V}_{11} = 40\ \text{V},\ V_{11} = 80\ \text{V},\ \bar{V}_{12} = 520\ \text{V},\ V_{12} = 1040\ \text{V}.$$

The output voltage of the first submultilevel converter ($V_{o,1}$), second submultilevel converter ($V_{o,2}$), and output voltage of cascade converter(V_{out}) of proposed 169-level topology is shown in Fig. 15. Based on this figure, it is clear that the output voltage of 169-level converter (V_{out}) is the sum of output voltage of the first submultilevel ($V_{o,1}$) and second submultilevel converters ($V_{o,2}$).

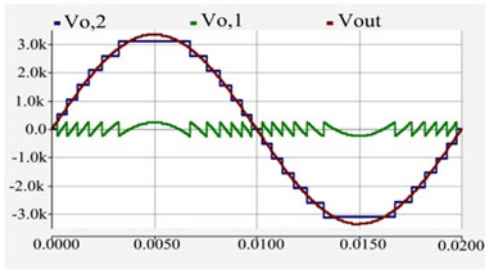

Fig. 15. Simulation results of output voltages of the first submultilevel ($V_{o,1}$), second submultilevel ($V_{o,2}$), and output voltage of cascade converter (V_{out}) in 169-level cascade converter.

IX. Conclusion

In this paper, a novel cascade multilevel converter was presented. The recommended cascade topology comprises of cascaded connection of submultilevel converters. Due to the extended feature of proposed topology, the proposed cascade converter was optimized to produce maximum levels with the least number of components. The optimum structures were compared with other topologies to prove the merits of recommended circuit. Based on comparison results, it was indicated that the proposed cascade topology needs minimum number of components and lower value of total blocking voltage of switches in comparison with binary and trinary CHB topologies and presented topologies in [9]–[16]. Simulation and experimental results were provided to verify the ability of presented submultilevel and cascade converters.

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