Optimised inverter by switch sharing: a control solution for photovoltaic applications

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Abstract: Switch-sharing-based multilevel inverter can be useful to develop an improved-performance DC–AC converter for low-power photovoltaic applications. However, this cannot be fully achieved without having a reliable control solution. Hence, this study presents a smart control strategy equipped with an adaptive proportional–integral controller. The adaptive characteristic is established through a tuning module that continuously fine tunes only one parameter. With the tuning mechanism, the load current quality is able to be continuously retained at the acceptable level even during the presence of disturbances. To validate the control performance, experimental work has been conducted on a laboratory prototype under load-disturbance conditions.

1 Introduction

Aspiration towards green growth has become the ultimate goal of many countries nowadays. Green growth emphasises the improvement of the quality of life without jeopardising the sustainability of the environment and natural resources. One strategy to realise this is to enhance the deployment of renewable energy including that originated from sunlight. In a photovoltaic (PV) system, an inverter is installed to convert DC power generated from the PV modules into AC power. In most cases, the inverter is required to carry out the conversion with less energy loss in order to attain high efficiency. In addition, the inverter is also expected to perform according to certain power quality standards.

In low-power PV applications, single-phase inverters are normally used. However, when the PV system is connected to the grid through single-phase inverters, a concern arises owing to the fact that a certain phase may have more such connections as compared with other phases in the three-phase network. Coupled with uneven distribution of single-phase loads among the three-phase power systems, voltage unbalance is typically observed as the result [1]. This phenomenon is undesirable as it causes instability to the power systems. As a consequence, this leads to more losses and heating effects, reduced efficiency and decreased life of motors, excessive current in one or two phases that can trip overload protection circuits, large voltage ripple in DC link and high reactive power for pulse-width-modulated rectifiers used in adjustable speed drives [2]. In addition, another shortcoming is that single-phase inverters are not able to transfer as much power as the three-phase inverters [3]. In contrast, the three-phase counterparts can produce a constant power when operated at unity power factor [4]. As a result, the DC-link voltage ripple is small enough that smaller DC-link capacitors can be used. This contributes to a reduction in cost, better reliability and higher lifetime for the PV systems [5].

In most cases, the commercial three-phase inverters for PV systems adopt the conventional two-level full-bridge topology [6]. In order to form a transformerless configuration for connection to the grid, some modifications are made to the topology, which result in the split DC-link concept and the four-leg structure [7]. To overcome the problems of the two-level inverters in maximising the power extracted, minimising the electromagnetic interference level, reducing the switching loss, lowering the harmonic distortions and decreasing the filter size, multilevel inverters have been introduced. There are various configurations to realise the three-phase multilevel circuits with the following three are the most common ones: flying capacitor, cascaded H-bridge and diode-clamped or neutral-point-clamped topologies [8–10]. The latest development shows that the last two topologies have attracted more attention for PV applications [3].

Although cascaded H-bridge and diode-clamped topologies have been used, they are not exactly suitable for low-power usage. In low-power applications, the inverter's voltage rating is not required to be way beyond the maximum voltage rating of the semiconductor power switches used in the inverter circuit. In other words, the voltage stress that each power switch has to withstand does not need to be mandatorily reduced and can be equal to the total DC-link voltage. Hence, the need for multilevel inverters is basically irrelevant as they will be underutilised. On the other hand, although the two-level full-bridge inverter is sufficient for these applications, it is not able to achieve higher efficiency as it has to operate at a very high switching frequency in order to meet the power quality requirements.

The weaknesses of the existing multilevel inverters and the full-bridge inverter can be resolved by using the switch-sharing-based multilevel inverter [11, 12]. The inverter is designed as a result of the optimisation made via switch-sharing approach to reduce circuit complexity. In some ways, the inverter can be seen as an extended version of the single-phase multilevel inverter presented in [13, 14]. The switch-sharing-based multilevel inverter is not only expected to perform as good as the cascaded H-bridge and diode-clamped inverters, but also can be fully utilised with better efficiency and output quality as compared with the full-bridge inverter. However, these advantages cannot be completely exploited if the control scheme does not work well to cope with disturbances. In this respect, current control schemes can play a vital role to produce good dynamic responses. There are many current control schemes found in the literature and these include hysteresis control [15], predictive control [16], voltage-oriented control [17] and direct power control (DPC) [18]. In search for better performance, at least two control methods have been combined [19–27].

Owing to the fast dynamic response and the absence of the synchronous rotating frame transformation [28], DPC scheme is adopted in this work. However, the conventional DPC scheme employs hysteresis controllers which contribute to the variation of
The circuit configuration of the switch-sharing-based multilevel inverter is shown in Fig. 1 [11]. It is a four-level structure with two bidirectional switches ($Q_{10}$ and $Q_{11}$) used for sharing among the three phases. Between the cascaded H-bridge and the diode-clamped topologies which have been gaining a lot of interest for PV applications, this inverter carries the most resemblance to the latter. Therefore, it is fair to use the diode-clamped inverter as reference for comparison in this analysis. The proposed inverter is compared with the three-level and four-level structures of the diode-clamped inverter in order to investigate its efficacy, from the perspectives of circuit complexity and overall performance.

2.1 Circuit complexity

Circuit complexity is commonly evaluated by the number of circuit components. It is an important criterion that is usually considered to form the first impression about a particular inverter. Besides providing estimation about the inverter’s volume and the level of control difficulty, circuit complexity also affects the cost of implementation that normally gives a strong impact on the viability of the inverter for a certain application. Table 1 presents the comparison of the component count and its expected level of impact on volume, control complexity and cost between the proposed inverter and the three-level and four-level diode-clamped inverters. It can be observed that the inverter offers the lowest number of power switches used, namely 11 in contrast to 12 and 18 employed in the three-level and four-level diode-clamped inverters, respectively. In terms of the total component count, the inverter records 40, which is higher by 25% when compared with the three-level diode-clamped inverter, but is lower by 21.6% when referring to the four-level diode-clamped inverter as the benchmark.

From the component count analysis, it can be inferred that the inverter provides a good balance between the three-level and four-level diode-clamped inverters as far as the following three perspectives are concerned: volume, control complexity and cost. Based on the component count, the volume occupied by the inverter can be deemed as acceptable. However, this is subjective, depending on the amount of space optimisation that has taken place when constructing the circuit. In terms of control complexity, the low number of power switches can be implied to result in low control complexity. However, since the inverter generates seven voltage steps in the line voltage waveforms, the complexity of the modulation algorithm can be comparable to that of the four-level diode-clamped inverter.

Factors such as the power range of a specific application can affect the cost of the circuit components. This cost is mostly contributed by the expenses for the power switches, since switches are more expensive than diodes. In addition, the ratings of the power switches also cause the cost to vary. The higher the ratings, the higher the cost is. If similar ratings are considered for the three inverters, the proposed inverter can offer the lowest power switch cost.

2.2 Performance

Table 2 presents the performance comparison between the inverter and the two diode-clamped inverters. It can be observed that the inverter shows better level-to-switch ratio, owing to the use of shared bidirectional switches. The power loss analysis that is based on the method presented in [12] indicates mixed data. The diode conduction loss of the inverter appears to be higher than those of the diode-clamped inverters. The same trend can be observed for the diode switching loss as well. However, this is effectively compensated by the considerable reduction in the insulated gate bipolar transistor (IGBT) conduction loss. IGBT is the type of power switch normally used in the inverter circuit. The IGBT switching loss shows a similarity among the three inverters.

From the overall perspective, for a comparable amount of output power, the proposed inverter generates lower power loss than that of the four-level diode-clamped inverter but higher power loss when compared with the three-level structure. This can be translated into an efficiency performance that is calculated at 94.7%. Although the efficiency is lower than that of the three-level

![Image](46x664 to 283x793)

**Table 1** Component count and impact investigation

<table>
<thead>
<tr>
<th>Components/impact perspective</th>
<th>Total number/impact level</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Three-level diode clamped</td>
</tr>
<tr>
<td>power switches</td>
<td>12</td>
</tr>
<tr>
<td>anti-parallel diodes</td>
<td>12</td>
</tr>
<tr>
<td>bidirectional switch diodes</td>
<td>0</td>
</tr>
<tr>
<td>clamping diodes</td>
<td>6</td>
</tr>
<tr>
<td>DC-link capacitors</td>
<td>2</td>
</tr>
<tr>
<td>total component count</td>
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</tr>
<tr>
<td>volume</td>
<td>small</td>
</tr>
<tr>
<td>control complexity</td>
<td>low</td>
</tr>
<tr>
<td>semiconductor cost</td>
<td>low</td>
</tr>
</tbody>
</table>

The circuit configuration of the switch-sharing-based multilevel inverter is presented in Section 3. Section 2 first provides an analysis of the strengths of the switch-sharing-based multilevel inverter. Section 4 then describes the details of the adaptive controller. Evaluation of the proposed control scheme via experimental investigations is given in Section 5. Finally, Section 6 summarises the conclusions.

2 Optimisation by switch sharing: an analysis
diode-clamped inverter, the inverter performs much better in terms of total harmonic distortion (THD) results. Hence, if the inverter is connected to the grid, the use of a small filter is then adequate. Since the filter cost is normally more expensive than the semiconductor cost, the inverter can offer a competitive total cost of implementation in comparison to those of the diode-clamped inverters particularly the three-level structure. This is made possible because of the fact that the three-level diode-clamped inverter may have high filter cost despite the low semiconductor cost it offers.

In conclusion, the proposed inverter basically combines the strong traits of the four-level and three-level diode-clamped inverters, while at the same time, reducing their drawbacks. It can still provide low THD output like what the four-level diode-clamped inverter can do and the three-level diode-clamped inverter cannot do, but at a cost that is comparable to that of the three-level diode-clamped inverter, of which the four-level diode-clamped inverter cannot achieve.

3 Proposed control topology

A good control strategy plays an important role in producing a good dynamic response in the wake of disturbances in order to maintain the best performance of the inverter. Fig. 2 portrays the proposed control topology that is based on DPC scheme with the use of PI controllers and a space vector modulator. In this work, the disturbance is represented by the load change. The three-phase currents and voltages at the load side are converted to stationary α–β reference frame quantities. These quantities are used to estimate the instantaneous active power \( p \) and reactive power \( q \). This is performed by applying the following:

\[
\begin{bmatrix}
  u_a \\
  u_b \\
  u_c
\end{bmatrix} = \frac{2}{\sqrt{3}} \begin{bmatrix}
  1 & -\frac{1}{2} & -\frac{1}{2} \\
  \frac{\sqrt{3}}{2} & -\frac{1}{2} & -\frac{1}{2} \\
  \frac{\sqrt{3}}{2} & -\frac{1}{2} & -\frac{1}{2}
\end{bmatrix} \begin{bmatrix}
  i_a \\
  i_b \\
  i_c
\end{bmatrix}
\]

\( u \) is a general variable to represent the voltage and current quantities. To obtain \( p \) and \( q \), the resulting voltage and current after the stationary frame transformation are used in the following equations [20, 29]:

\[
\begin{align*}
  p &= v_d i_d + v_b i_b \\
  q &= v_d i_q + v_b i_q
\end{align*}
\]

The estimated \( p \) and \( q \) are then compared with their respective references \( p_{ref} \) and \( q_{ref} \). The power errors \( \Delta p \) and \( \Delta q \) are next fed to the PI controllers to produce digitised signals \( v_{s,d} \) and \( v_{s,q} \) through a decoupling network [30]. This is done by first getting the DC quantities of the voltage and current in the synchronous rotating \( d-q \) frame using the following:

\[
\begin{bmatrix}
  u_d \\
  u_q
\end{bmatrix} = \begin{bmatrix}
  \cos(\omega t) & \sin(\omega t) \\
  -\sin(\omega t) & \cos(\omega t)
\end{bmatrix} \begin{bmatrix}
  i_d \\
  i_q
\end{bmatrix}
\]

\( \omega \) is the angular frequency of the rotating frame. \( v_{s,d} \) and \( v_{s,q} \) are the results of the decoupling network represented by the equations below:

\[
\begin{align*}
  v_{s,d} &= v_d - \omega L f i_q + \Delta v_d \\
  v_{s,q} &= \omega L f i_d + \Delta v_q
\end{align*}
\]

\( L_f \) is the inductance of the filter. \( \Delta v_d \) and \( \Delta v_q \) are the output quantities as a result of the PI controllers which are defined as follows:

\[
\begin{align*}
  \Delta v_d &= k_{p,d} \Delta p + k_{i,d} \int \Delta p dt \\
  \Delta v_q &= k_{p,q} \Delta q + k_{i,q} \int \Delta q dt
\end{align*}
\]
\[ \Delta v_q = k_{p,q} \Delta q + k_{i,q} \int \Delta q dt \]  

(8)

\[ \Delta v_d = k_{p,d} \Delta d + k_{i,d} \int \Delta d dt \]  

(9)

\[ \Delta v_d, \Delta v_q \] are the proportional and integral gains of the real power controller whereas \( k_{p,q} \) and \( k_{i,q} \) are those for the reactive power controller. Transformation of \( v_{s,d} \) and \( v_{s,q} \) to the \( \alpha-\beta \) frame is required before the modulator can generate the switching signals. This is realised using the following equation:

\[ v_{s,d} = \frac{\cos(\omega t) - \sin(\omega t)}{\sin(\omega t)} v_{s,q} \]  

From these quantities, the magnitude and angle of the reference voltage vector can be computed using the following:

\[ V_{ref} = \sqrt{v_{s,d}^2 + v_{s,q}^2} \]  

(10)

\[ \theta_{ref} = \tan^{-1}\left( \frac{v_{s,q}}{v_{s,d}} \right) \]  

(11)

By using the modified space vector pulse width modulation technique proposed in [11], the appropriate switching signals can be generated.

4 Adaptive controller

It can be seen from Fig. 2 that there are two PI controllers employed, one of the conventional type and the other is made adaptive. In this work, the conventional PI controller is configured for \( q \) control and the adaptive controller is meant to handle \( p \). This is adopted since in this investigation, the load disturbance is introduced in the manner that will not cause a step change in \( q \). This is realised by having a constant power factor of the load so that \( q_{ref} \) can be kept at a fixed value. This practice is normal especially in grid-connected PV systems that usually require a unity power factor operation. Since \( q_{ref} \) is constant, the use of a conventional controller is sufficient to control \( q \). The case is different for \( p \) whereby \( p_{ref} \) varies according to the magnitude of the load change. Therefore, an adaptive controller is necessary. The adaptive feature is derived from the tuning module included in the controller's structure with only one parameter is involved for tuning.

4.1 Anti-windup module

The performance of the PI controller is very much influenced by the load parameters. At a constant load condition, the PI controller can only receive its input within an allowable range, beyond which the input becomes constant as it reaches the saturation level. This is so since the controller's input is actually derived from the output of a closed-loop system whose values are restricted by the load parameters. Therefore, when the controller's input has reached saturation, this means that the system's output has arrived at its maximum or minimum restricted value. Although saturation has been reached, the integral part of the controller continues to increase or decrease which causes the controller's output to increase or decrease as well. At this stage, the change in the controller's output has no more effects on the system's output since the maximum or minimum restricted value has already been achieved. If the integral component of the controller keeps integrating, this causes the controller to experience integral windup effect. As a consequence, the controller may take a long time to achieve the steady-state condition.

To avoid the windup effect, the controller is equipped with two anti-windup modules. One module is to limit the output of the integrator and the other is to set proper bounds for the controller's output. In reference to the adaptive controller that controls \( p \), with the anti-windup modules included, the integral term \( \Delta v_{d,i} \) in (7) is governed by the following conditions:

\[ \Delta v_{d,i} = k_{p,d} \Delta d + k_{i,d} \int \Delta d dt, \]  

if \( m_{low} \leq \Delta v_d \leq m_{high} \)  

(12)

\[ \Delta v_{d,i} = m_{low}, \]  

if \( \Delta v_d < m_{low} \)  

(13)

\[ \Delta v_{d,i} = m_{high}, \]  

if \( \Delta v_d > m_{high} \)  

(14)

As for the controller's output \( \Delta v_q \), the following conditions apply:

\[ \Delta v_q = k_{p,q} \Delta q + k_{i,q} \int \Delta q dt, \]  

if \( n_{low} \leq \Delta v_q \leq n_{high} \)  

(15)

\[ \Delta v_q = n_{low}, \]  

if \( \Delta v_q < n_{low} \)  

(16)

\[ \Delta v_q = n_{high}, \]  

if \( \Delta v_q > n_{high} \)  

(17)

\( m_{low} \) and \( m_{high} \) are the minimum and maximum limits of the integral anti-windup module and \( n_{low} \) and \( n_{high} \) are the bottom and top bounds of the controller's anti-windup module. With suitable values of \( m_{low}, m_{high}, n_{low} \) and \( n_{high} \), the controller's performance can be further improved since it is in a better position to run at its optimum operating point for a particular load condition.

4.2 Proposed tuning algorithm

It is commonly observed that the performance of the PI controller is somehow compromised when there is a change in the load condition. The degree of the performance drop depends on the amount of the load change. If the load change is small enough, the controller's good performance can still be maintained. However, when the amount of load change is significant, the controller may not be able to run at its optimum operating point anymore and as a result, its performance considerably deteriorates. Here, optimum operating point is said to be reached when the load current of the inverter reaches the desired range of the THD value, namely <5%. Beyond this optimum point, the load current quality may worsen. Hence, parameter tuning is normally carried out to make the controller adaptive so that proper adjustment can be made to suit the different load conditions. Many tuning methods can be found from the literature, such as stochastic multi-parameters divergence optimisation [31, 32], simultaneous perturbation stochastic approximation [33, 34] and artificial-intelligence-based optimisation [35, 36]. In most cases, the tuning is concentrated more on the proportional and integral gains. In this work, a different perspective is viewed in which the anti-windup parameter is the one focused for tuning.

From Fig. 2, the proposed adaptive controller consists of an additional module known as the tuning module. For the module to work, it requires two reference signals and a feedback signal from the output of one of the processes involved in the system. The two reference signals are \( p_{ref} \) and the desired reference voltage vector amplitude, \( V_{target} \). The feedback signal is \( V_{ref} \). The purpose of the tuning module is to maintain or even improve the quality of the load current after a change in the load condition. This is realised by applying an additional criterion for the controller to achieve namely \( V_{target} \). \( V_{target} \) is chosen based on certain preferred characteristics such as low-voltage THD or good voltage harmonic spectrum. The selection of \( V_{target} \) can be made within a range between 0 and 100%, in which 100% refers to the highest reference voltage vector amplitude allowed before overmodulation occurs. According to [11], it is observed that a reference voltage vector of amplitude 70% and higher produces good THD and harmonic spectrum for the four-level switch-sharing-based inverter.

The tuning algorithm is designed to direct \( V_{ref} \) to be as close as possible to \( V_{target} \) by adjusting \( n_{low} \) only at the controller's anti-windup module without modifying other parameters including the proportional or integral gains. This is to ensure that the convergence of \( V_{ref} \) results in the achievement of the optimum operating point. Adjustment of the bottom bound expands or shrinks the allowable range of the anti-windup module so that the
controller’s output $\Delta V_f$ does not reach saturation and $\Delta V_f$ value is not replaced by the bound, for a particular load condition. By removing the cause that can lead to $\Delta V_f$ reaching saturation, it increases the controller’s ability to find the most appropriate operating point within the newly defined operating region. The process flow of the tuning mechanism as displayed in Fig. 3 is explained as follows:

i. The current value of $p_{ref}$ [denoted as $p_{ref(current)}$] and the most recently stored previous value of $p_{ref}$ [represented by $p_{ref(previous)}$] are compared.

ii. If the two values are different, $p_{ref(previous)}$ is updated with the value of $p_{ref(current)}$. $n_{low}$ is then calculated according to the following:

$$n_{low(current)} = X e^{V_{rho}} + Y e^{W_{rho}}$$

(18)

$V_{rho}$ and $W_{rho}$ are constants.

iii. If the two values are similar, $V_{ref}$ is compared with $V_{target(top)}$ and $V_{target(bottom)}$. Both are defined as follows:

$$V_{target(top)} = V_{target} + l$$

(19)

$$V_{target(bottom)} = V_{target} - l$$

(20)

$l$ is a constant denoting the allowable tolerance between $V_{target}$ and $V_{ref}$. $l$ can be taken as 1–2% of $V_{target}$.

iv. If $V_{ref}$ is higher than $V_{target(top)}$, $n_{low(current)}$ is determined by reducing the previous state of $n_{low}$ [$n_{low(previous)}$] by a fixed value $Z$ as follows:

$$n_{low(current)} = n_{low(previous)} - Z$$

(21)

v. If $V_{ref}$ is lower than $V_{target(bottom)}$, $n_{low(current)}$ is determined by increasing the previous state of $n_{low}$ [$n_{low(previous)}$] by a fixed value $Z$

$$n_{low(current)} = n_{low(previous)} + Z$$

(22)

vi. Steps (i)–(v) are repeated until $V_{ref}$ lies within the allowable tolerance around $V_{target}$.

As stated in step (ii), $V$, $W$, $X$ and $Y$ are constants that need to be found. Determination of these constants is carried out through a preliminary experiment. In the experiment, for different values of $p_{ref}$ which are set according to the amount of the load given, $n_{low}$ is determined via a trial-and-error method. Selection of $n_{low}$ is made based on the lowest THD of the load current, measured using a power analyser. Low THD implies high quality of the current. Based on the data of $p_{ref}$ and $n_{low}$ obtained from the experiment, actual $n_{low}$–$p_{ref}$ curve can be plotted. An equation based on (18) that can approximately represent the actual curve can be derived using MATLAB curve-fitting tool. From the derived equation, constants $V$, $W$, $X$ and $Y$ can be obtained. On the other hand, determination of $Z$ depends on the actual implementation of the controller. If digital implementation is adopted, the speed of the digital processor and the sampling time are to be considered before the suitable value of $Z$ is selected. This is to avoid slow and undesired controller response.

5 Experimental validation

5.1 Hardware set-up

To validate the control strategy experimentally, a workable hardware set-up is then prepared. It basically consists of the DC input source, the load bank and the inverter prototype. Figs. 4 and 5 show the complete hardware set-up used in this work. The DC source is provided by three nickel-metal hydride (NiMH) batteries which represent the PV source. Each battery is of 48 V, 13 Ah capacity. It should be noted that the essence of the control strategy does not change despite the PV source is emulated by batteries. The load bank is of a variable three-phase RL type (resistive-inductive) with Y-connection. Filtering inductors of 10 mH per phase are also placed between the inverter prototype and the load.

The inverter prototype is composed of two main sections namely the hardware and software parts. The hardware part is related to the construction of the power circuit of the inverter. The control part is provided by the software module. The power circuit is constructed using semiconductor devices. Eleven units of IGBT IRG4PC40UDPFb are used as switches. Diodes RHRP30120 are
used to build the bidirectional switches. RC (resistive–capacitive) snubber is also connected across each IGBT to prevent voltage surges during turning off and to reduce electromagnetic interference. Besides, auxiliary circuits such as gate drives and dead band generators are included to complete the power circuit. The gate drives provide isolation between the power circuit and the control unit for protection purposes, and also increase the voltage level of the switching signals to that acceptable for the IGBTs to operate. The dead band generators produce a blanking time of 1 μs to avoid a short circuit across the DC sources. To measure the voltages and currents for the control unit to use as inputs, voltage and current sensors are used.

The control unit consists of two digital signal processor (DSP) boards of model eZdspTM F2812. The processor is of 32-bit, fixed-point type with 150 million instructions per second operating speed. Besides the processor, the board is also accompanied with specialised features which are suitable to develop control algorithms for real-time applications. Among those features which are useful include general purpose input/output ports, analogue-to-digital conversion (ADC) module and event manager timers. For the purpose of building and debugging the program code in C language platform, a software package known as Code Composer Studio is employed. To facilitate the programming for the two boards, two host computers are used.

The two DSP boards are used to act as the modulator and the controller. The reason to use two DSP boards is to separate the program code for the switching signal generation, from the code that executes ADC results reading, parameter transformation and PI controller functions. By doing so, long program code that leads to the reduction of the program execution speed can be avoided. The sampling frequency is set at 4.9 kHz as this is the maximum frequency that can be achieved by the processor to ensure distortion-free switching signals. To facilitate communication between the modulator and the controller, a simple data communication interface is developed based on flag signalling approach.

5.2 Results and discussions
The purpose of the experiment is to verify that the control strategy produces better results when the adaptive controller with the proposed tuning algorithm is employed. Before performing this verification, an appropriate value of $V_{\text{target}}$ needs to be determined. For this purpose, a curve showing the relationship between the voltage THD and the reference voltage vector amplitude is plotted,
as displayed in Fig. 6. It can be observed that 80% amplitude records the lowest THD. Hence, \(V_{\text{target}}\) can be set at this amplitude. Once the value of \(V_{\text{target}}\) has been finalised, the experiment for the aforementioned verification can be conducted. In order to do this, the experiment is conducted in two situations. In the first situation, the experiment is carried out with the adaptive controller included in the control strategy to control \(p\). In the second situation, the adaptive controller is replaced with the conventional PI controller with no tuning module applied. For the tuning algorithm to function as desired, early test is carried out to collect \(n_{\text{low}}\) data for different values of \(p_{\text{ref}}\) at a load power factor of 0.82. The result of the test is presented graphically in Fig. 7. The broken line in the figure represents the actual data collected. The full line indicates the equation that can approximately represent the actual data. By applying the procedure mentioned in Section 4.2, the aforementioned equation that is based on (18) is derived. The equation is presented as follows:

\[
n_{\text{low}} = (1.062 \times 10^{-11} e^{0.06087p_{\text{ref}}}) + 4.442 e^{0.00426p_{\text{ref}}}
\]  

(23)

From (23), the constants are identified as below:

\[
V = 0.06087, \ W = 0.00426, \ X = 1.062 \times 10^{-11} \quad \text{and} \quad Y = 4.442
\]

(24)

Since \(X\) is too small, it can be ignored. Hence, (23) is simplified to

\[
n_{\text{low}} = 4.442 e^{0.00426p_{\text{ref}}}
\]

(25)

In addition, other constants used for digital implementation of the controller are given in Table 3. They are first determined by using the simulation model developed on MATLAB platform. Unlike actual implementation, the simulation model assumes an ideal condition without considering real factors such as processor's speed and sampling time. Hence, further adjustment is made via trial-and-error method to arrive at the appropriate values. However, this adjustment is done one time only. All values are then set fixed except \(n_{\text{low}}\) which is adjusted using the tuning scheme.

The experimental results showing the step responses as a result of the load changes when the tuning mechanism is applied are portrayed in Fig. 8. Fig. 8a shows the step-up response when the load reduces from 62.0 to 15.6 \(\Omega\) while Fig. 8b indicates the step-down response when the load increases by the same amount. To further illustrate the improvement made by the proposed tuning, the experimental results with and without tuning during transient situations are given in Figs. 9a and 9b.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Z)</td>
<td>0.05</td>
</tr>
<tr>
<td>(l)</td>
<td>0.01</td>
</tr>
<tr>
<td>(m_{\text{high}})</td>
<td>10.0</td>
</tr>
<tr>
<td>(m_{\text{low}})</td>
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<tr>
<td>(n_{\text{high}})</td>
<td>150.0</td>
</tr>
<tr>
<td>(k_{p,d})</td>
<td>100.0</td>
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<tr>
<td>(k_{p,q})</td>
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<tr>
<td>(k_{i,d})</td>
<td>100.0</td>
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<tr>
<td>(k_{i,q})</td>
<td>10.0</td>
</tr>
</tbody>
</table>

Table 3 Parameter values of the controller
and steady-state conditions are provided in Figs. 9 and 10, respectively. The tuning module employed in the control scheme results in the rise of $n_{\text{low}}$ from 8.6 to 28.6 during the load reduction. For the case with tuning, the tracking performance is satisfactory and the load current quality is maintained with the THD after the load change is recorded at 1.96%. The rise time, peak time and settling time are measured as 13, 21 and 35 ms, respectively. The per cent overshoot is calculated as 44.4%. The inverter output voltage remains the same before and after the load change.

On the other hand, the results without tuning indicate poor tracking performance. The load current also records higher THD after the load change namely 5.18%. Although the response records shorter rise time and peak time namely, 8 and 12 ms, respectively, it takes longer time to achieve the steady state (60 ms), which is about double the settling time recorded for the case when the tuning module is included. The per cent overshoot is very big, calculated as 150%. The inverter output voltage waveform also appears to be different after the load change. In terms of the power error, both cases show similar amplitude. The amplitude is as a result of the filter's inductance value used. It can be further reduced with the use of a bigger inductance value. All in all, the results reveal the effectiveness of the proposed adaptive controller with the suggested tuning mechanism in maintaining the good performance of the inverter to produce good quality of the load current, even during the presence of disturbances.
6 Conclusions
An improved control strategy for the switch-sharing-based multilevel inverter suitable for PV applications has been presented in this paper. The strategy is based on the DPC scheme with the use of PI controllers and a space vector modulator. The improvement is reflected through the utilisation of an adaptive PI controller with a tuning module to control \( p \) as \( \text{Pref} \) varies when load disturbances occur. The proposed tuning method enhances the controller's ability to produce good quality of the load current even during disturbances via the tuning of one anti-windup parameter only. Such control method can also be extended to the grid-connected PV systems by making \( \text{Pref} \) to be responsive to the grid voltage disturbances instead. Besides, with zero \( \text{Pref} \) a unity power factor operation can be achieved too. The performance of the proposed control strategy has been experimentally assessed and the results show that the desired outputs have been fully accomplished.

7 Acknowledgment
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8 References