Optimal Design of New Cascaded Switch-Ladder Multilevel Inverter Structure

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***Abstract*—In this paper, a new cascade switch-ladder multilevel inverter topology is presented which can generate a large number of output voltage levels. First, a fundamental switch-ladder multilevel inverter structure is described. Then, the structure of recommended cascade topology based on series connection of fundamental switch-ladder topologies is presented. To generate maximum number of levels with minimum number of switching elements, dc sources, and voltage on switches, the proposed cascade topology is optimized. Comparison results prove that the presented cascade topology requires fewer numbers of components. Also, the value of voltage rating on switches is less than other structures. Experimental results for two topologies are analyzed to verify the performance of the proposed topology.**

***Index Terms*—Bidirectional switch, components, multilevel inverter, optimization, voltage on switches.**

I. Introduction

DUE to the enormous applications of multilevel inverters in renewable energy systems, machine drives, and FACTS devices, the researchers have been improving the structures of multilevel inverters in terms of reduction of components and voltage rating on switches [1]–[3]. Compared to the two-level inverter, multilevel inverters have numerous advantages such as lower values of voltage on switches, total harmonic distortion (THD), electromagnetic interference, etc. For high-voltage applications, the modular multilevel converter (MMC) has been presented. The switching losses of MMC topology is low and its extension is simple. However, this structure uses many switches and dc capacitors [4], [5].

In 1970, the first topology for multilevel inverter was proposed which was called cascade H-bridge (CHB) [6]. In 1981, the second proposed multilevel inverter by Nabae was named neutral-point-clamped (NPC). Due to the series connection of input capacitors, there is an inherent challenge in voltage unbalance of capacitors [7], [8]. An alternative topology for NPC is a flying capacitor (FC). As the number of levels goes up, the number of capacitors and switches increases in the FC topology. Also, voltage balancing of capacitors is another demerit of this topology [9]–[11]. For the CHB topology, several algorithms were recommended to determine the values of sources [12]–[15]. The presented trinary algorithm in [15] generates the levels with minimum components.

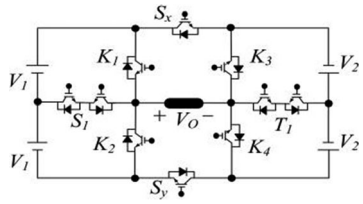

Fig. 1. Presented basic unit structure.

Researchers have been trying to propose new multilevel inverters that require the least number of switches, drivers, and dc sources. Also, reduction of voltage rating on switches has been done. In [16]–[18], new basic structures for multilevel inverter have been presented. The number of IGBTs, drivers, and the voltage on the switches in these topologies is high.

Other cascaded topologies have been recommended in [19]–[23]. The proposed topology in [19] uses many IGBTs and the value of total voltage on switches is high. However, the number of drivers is lower than other topologies. As the number of levels goes up, the bus bar topologies of multilevel dc-link converters will be complex and difficult to fabricate and voltage balancing. To overcome these problems, a new family of modular matrix converter was proposed. These topologies can regulate the voltage frequency and magnitude, while operating with arbitrary power factors [24], [25]. However, the proposed topologies in [10]–[23] cannot regulate the amplitude and frequency of the output voltage.

In this study, a new structure for cascade multilevel inverter is introduced, which needs minimum number of elements in comparison with the presented structures in [10]–[23].

II. Proposed Fundamental Multilevel Inverter

The structure of the proposed basic unit is presented in Fig. 1. This circuit consists of six unidirectional switches $(K_1, K_2, K_3, K_4, S_x, S_y)$, two bidirectional switches (S_1, T_1), and four dc sources. Two of the dc sources have the same magnitude of V_1 and the value of the two other sources is V_2. The switching states of basic unit to generate all levels are provided in Table I. To increase the number of

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TABLE I
SWITCHING STATES OF THE PROPOSED BASIC UNIT

No.	Switches States								V_O
	K_1	K_2	K_3	K_4	S_1	T_1	S_x	S_y	
1	1	0	1	0	0	0	1	0	0
2	0	0	0	1	1	0	0	1	V_1
3	0	0	1	0	1	0	1	0	$-V_1$
4	0	1	0	0	0	1	0	1	V_2
5	1	0	0	0	0	1	1	0	$-V_2$
6	1	0	0	1	0	0	0	1	$2V_1$
7	0	1	1	0	0	0	1	0	$-2V_1$
8	0	1	1	0	0	0	0	1	$2V_2$
9	1	0	0	1	0	0	1	0	$-2V_2$
10	0	0	0	0	1	1	0	1	V_1+V_2
11	0	0	0	0	1	1	1	0	$-(V_1+V_2)$
12	1	0	0	0	0	1	0	1	$2V_1+V_2$
13	0	1	0	0	0	1	1	0	$-(2V_1+V_2)$
14	0	0	1	0	1	0	0	1	V_1+2V_2
15	0	0	0	1	1	0	1	0	$-(V_1+2V_2)$
16	1	0	1	0	0	0	0	1	$2V_1+2V_2$
17	0	1	0	1	0	0	1	0	$-(2V_1+2V_2)$

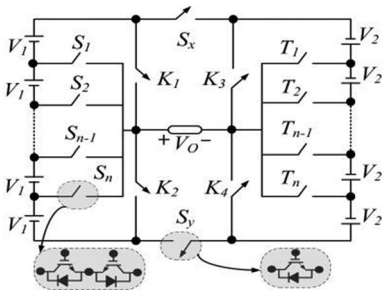

Fig. 2. Proposed fundamental switch-ladder multilevel inverter.

levels, the presented basic unit can be extended as shown in Fig. 2. The proposed extended basic unit is called fundamental switch-ladder multilevel inverter (FSLMI). To have a safe operation in the FSLMI, all the switches $S_1, S_2, \ldots, S_n$ and $T_1, \ldots, T_{n-1}, T_n$ should not be turned OFF at the same time because the FSLMI does not have a freewheeling path. It causes severe voltages to appear across the devices. Therefore, only one switch should be turned ON. Then, a delay time is considered between the switches.

III. PROPOSED CASCADE SWITCH-LADDER MULTILEVEL INVERTER (CSLMI)

A significant criticism of the proposed FSLMI, particularly those with higher levels, is that the increased component counts make the system bulky, costly, and complex. Also, the voltage rating on the switches of S_x and S_y is equal to the sum of all sources values. To reduce the number of used components and voltage on S_x and S_y, cascade topology based on series connection of m FSLMIs is recommended which is presented in Fig. 3 and is named cascade switch-ladder multilevel inverter (CSLMI). The output voltage of CSLMI (V_{out}) is equal to the sum of output voltages of the all FSLMIs. Then,

$$V_{\text{out}} = V_{o1} + V_{o2} + \ldots + V_{\text{om}}. \tag{1}$$

The circuit of the first, second, ..., and mth FSLMI consists of $2n_1$, $2n_2$, ..., and $2n_m$ bidirectional switches as a ladder,

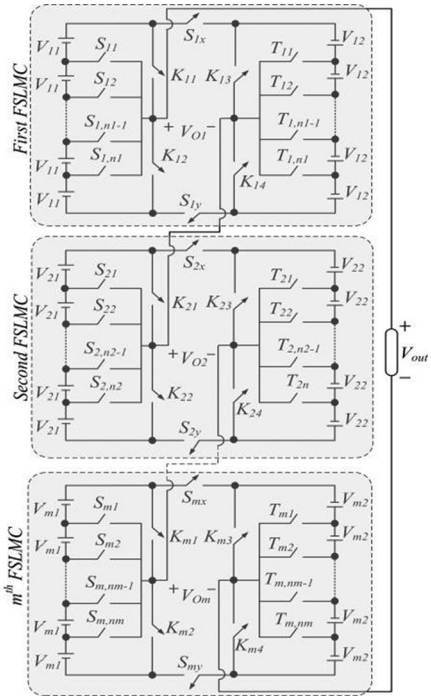

Fig. 3. Proposed cascade switch-ladder multilevel inverter.

respectively. To obtain the maximum number of levels with constant number of power electronic elements, we have to consider that the number of bidirectional switches in each FSLMI is equal. In other words

$$2n_1 = 2n_2 = \cdots = 2n_m = 2n. \tag{2}$$

Two algorithms are described for determining the values of sources of CSLMI structure as follows.

A. First Algorithm

In this algorithm, the values of sources in each FSLMI are similar. However, the values of sources in various FSLMIs are nonequal and are obtained using the following equations.

First FSLMI:

$$V_{11} = V_{12} = V_{\text{dc}}. \tag{3}$$

Then, the maximum amplitude of the output voltage in the first FSLMI $(V_{o1,\max})$ will be

$$V_{o1,\max} = (n+1)(V_{11} + V_{12}). \tag{4}$$

Second FSLMI:

$$V_{21} = V_{22} = 2(V_{o1,\max}) + V_{\text{dc}}. \tag{5}$$

Using (3)–(5), it is clear that

$$V_{21} = V_{22} = (4n+5)V_{\text{dc}}. \tag{6}$$

The maximum amplitude of the output voltage in the second FSLMI $(V_{o2,\max})$ is obtained as follows:

$$V_{o2,\max} = (n+1)(V_{21} + V_{22}). \tag{7}$$

Third FSLMI:

$$V_{31} = V_{32} = 2(V_{o1,\max} + V_{o2,\max}) + V_{\rm dc}. \quad (8)$$

Substituting (4) and (7) in (8), we have

$$V_{31} = V_{32} = (4n+5)^2 V_{\rm dc}. \quad (9)$$

The maximum output voltage of the third FSLMI ($V_{o3,\max}$) is

$$V_{o3,\max} = (n+1)(V_{31} + V_{32}). \quad (10)$$

*For the m*th *FSLMI*:

$$V_{m1} = V_{m2} = (4n+5)^{m-1}.V_{\rm dc}. \quad (11)$$

Then, the number of produced levels of the first algorithm ($N_{\rm level,FA}$) can be calculated as follows:

$$N_{\rm level,FA} = (4n+5)^m. \quad (12)$$

B. Second Algorithm

In contrast to the described first algorithm, the values of dc sources of each FSLMI are nonequal in the second algorithm. In fact, the dc sources amplitudes of each FSLMI topology have two different values which are determined as follows:

First FSLMI:

$$V_{11} = V_{\rm dc} \quad (13)$$

$$V_{12} = (n+2)V_{\rm dc}. \quad (14)$$

The maximum output voltage of the first FSLMI ($V_{o,1,\max}$) is

$$V_{o1,\max} = (n+1)(V_{11} + V_{12}). \quad (15)$$

Second FSLMI:

$$V_{21} = 2(V_{o1,\max}) + V_{\rm dc} = (2n^2+8n+7)V_{\rm dc} \quad (16)$$

$$V_{22} = (n+2)V_{21}. \quad (17)$$

The maximum output voltage in the second FSLMI ($V_{o,2,\max}$) is

$$V_{o2,\max} = (n+1)(V_{21} + V_{22}). \quad (18)$$

Third FSLMI:

$$V_{31} = 2(V_{o1,\max} + V_{o2,\max}) + V_{\rm dc}. \quad (19)$$

Using (15), (18), and (19), we have

$$V_{31} = (2n^2+8n+7)^2 V_{\rm dc}. \quad (20)$$

Then, V_{32} is calculated as follows:

$$V_{32} = (n+2)V_{31}. \quad (21)$$

The maximum output voltage of the third FSLMI ($V_{o3,\max}$) is

$$V_{o3,\max} = (n+1)(V_{31} + V_{32}). \quad (22)$$

*m*th *FSLMI*:

$$V_{m1} = (2n^2+8n+7)^{m-1} V_{\rm dc} \quad (23)$$

$$V_{m2} = (n+2)V_{m1}. \quad (24)$$

Considering (13)–(24), the number of generated levels of the proposed second algorithm ($N_{\rm level,SA}$) is

$$N_{\rm level,SA} = (2n^2+8n+7)^m. \quad (25)$$

Using (2), the number of IGBTs ($N_{\rm IGBT}$), drivers ($N_{\rm driver}$), and sources ($N_{\rm source}$) in the CSLMI are computed as follows:

$$N_{\rm IGBT} = m(4n+6) \quad (26)$$

$$N_{\rm driver} = m(2n+6) \quad (27)$$

$$N_{\rm source} = m(2n+2). \quad (28)$$

IV. Evaluation of Total Maximum Voltage Rating on Switches of the Proposed CSLMI Structure

The maximum voltage rating on a switch is an important parameter which affects the inverter cost. To calculate the total maximum voltage on switches in CSLMI ($\rm TMVR_{sw}$), we have

$$\rm TMVR_{sw} = TMVR_{usw} + TMVR_{bsw}. \quad (29)$$

In this equation, $\rm TMVR_{usw}$ and $\rm TMVR_{bsw}$ are the total maximum voltage rating on unidirectional and bidirectional switches, respectively. $\rm TMVR_{usw}$ is computed as follows:

$$\rm TMVR_{usw} = \sum_{i=1}^{m} (V_{S_{ix}} + V_{S_{iy}} + V_{K_{i1}} + V_{K_{i2}} + V_{K_{i3}} + V_{K_{i4}}) \quad (30)$$

where $V_{S_{ix}}, V_{S_{iy}}, V_{K_{i1}}, V_{K_{i2}}, V_{K_{i3}}, V_{K_{i4}}$ are the values of the voltage on the unidirectional switches of $S_{ix}, S_{iy}, K_{i1}, K_{i2}, K_{i3}, K_{i4}$ in the *i*th FSLMI, respectively. To calculate $\rm TMVR_{usw}$, the maximum voltage rating of unidirectional switches in the *i*th FSLMI ($i = 1, 2, \ldots, m$) are computed. Then, the obtained calculations can be applied for other FSLMIs. In other words

$$V_{S_{ix}} = V_{S_{iy}} = (n+1)(V_{i1} + V_{i2}) \quad (31)$$

$$V_{K_{i1}} = V_{K_{i2}} = (n+1)V_{i1} \quad (32)$$

$$V_{K_{i3}} = V_{K_{i4}} = (n+1)V_{i2}. \quad (33)$$

Hence, using (30)–(33), the $\rm TMVR_{usw}$ of the proposed CSLMI topology can be easily computed as follows:

$$\rm TMVR_{usw} = 4\sum_{i=1}^{m} (n+1)(V_{i1} + V_{i2}). \quad (34)$$

It is clear that

$$\sum_{i=1}^{m} (n+1)(V_{i1} + V_{i2}) = \frac{N_{\rm level} - 1}{2}.V_{\rm dc}. \quad (35)$$

Using (34) and (35), $\rm TMVR_{usw}$ can be simplified as follows:

$$\rm TMVR_{usw} = 2(N_{level} - 1).V_{dc}. \quad (36)$$

To compute $\rm TMVR_{bsw}$, we have

$$\rm TMVR_{bsw} = \sum_{j=1}^{n}\sum_{i=1}^{m} (V_{S_{ij}} + V_{T_{ij}}) \quad (37)$$

where $V_{S_{ij}}$ and $V_{T_{ij}}$ are the values of voltage rating on the switches S_{ij} and T_{ij} in the *j*th bidirectional switch of the *i*th

FSLMI. Equation (37) can be rewritten as follows:

$$\mathrm{TMVR}_{\mathrm{bsw}} = G \times \left[\sum_{i=1}^{m} (V_{i1} + V_{i2})\right]. \tag{38}$$

In the above equation, G is computed as follows:

$$\begin{aligned} G &= 2\left[n + (n-1) + \ldots + \left(n - \frac{(n-3)}{2}\right)\right] + \frac{n+1}{2} \\ &= \frac{3n^2 + 2n - 1}{4} \quad \text{For odd } n \\ G &= 2\left[n + (n-1) + \ldots + \left(n - \frac{(n-2)}{2}\right)\right] \\ &= \frac{3n^2 + 2n}{4} \quad \text{For even } n. \end{aligned} \tag{39}$$

Considering (35), we have

$$\sum_{i=1}^{m} (V_{i1} + V_{i2}) = \frac{N_{\mathrm{level}} - 1}{2(n+1)}.V_{\mathrm{dc}}. \tag{40}$$

Using (38)–(40), $\mathrm{TMVR}_{\mathrm{bsw}}$ can be simplified as follows:

$$\mathrm{TMVR}_{\mathrm{bsw}} = \frac{G(N_{\mathrm{level}} - 1)}{2(n+1)}.V_{\mathrm{dc}}. \tag{41}$$

Then, considering (29), (36), and (41), $\mathrm{TMVR}_{\mathrm{sw}}$ will be

$$\mathrm{TMVR}_{\mathrm{sw}} = \left[2 + \frac{G}{2(n+1)}\right] \times (N_{\mathrm{level}} - 1) \times V_{\mathrm{dc}}. \tag{42}$$

As mentioned before, the voltage rating on the switches S_x and S_y are high in the structure of FSLMI topology and is equal to the sum of all sources values. This leads to restriction on the high-voltage applications. However, the proposed CSLMI topology utilizes multiple FSLMIs and the voltage on the switches S_{ix} and S_{iy} in the ith FSLMI is related to the sum of sources values of only the ith FSLMI. Therefore, the proposed CSLMI topology can be used in high-voltage applications. The current rating of switches is another important parameter in the design of a converter. In the proposed topology, when the switches are turned OFF, the current tend to be zero. However, when the switches are turned ON, the maximum current of the switches are equal to the load current.

V. Optimization of the Proposed CSLMI Topology

The proposed CSLMI topology comprises of cascaded connection of extended FSLMIs. To attain the maximum number of output voltage levels with minimum number of IGBTs, drivers, dc sources, and minimum value of voltage on switches, the CSLMI structure is optimized.

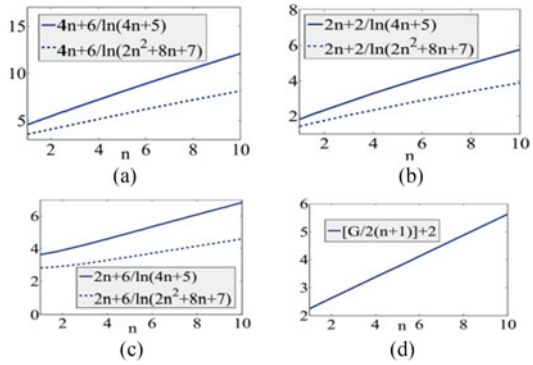

Fig. 4. Related curves to optimize the proposed structure in terms of minimizing (a) IGBTs, (b) dc sources, (c) drivers, (d) voltage rating on switches for constant number of levels to obtain parameter n.

A. Minimizing the Number of IGBTs for Constant Levels

Using (12), (25), and (26), N_{IGBTs} based on the proposed first and second algorithms are calculated as follows:

$$N_{\mathrm{IGBT}} = \ln\left(N_{\mathrm{level,FA}}\right) \times \frac{(4n+6)}{\ln(4n+5)} \tag{43}$$

$$N_{\mathrm{IGBT}} = \ln(N_{\mathrm{level,SA}}) \times \frac{(4n+6)}{\ln(2n^2+8n+7)} \tag{44}$$

where $N_{\mathrm{level,FA}}$ and $N_{\mathrm{level,SA}}$ are constant. Thus, N_{IGBT} is minimized when $\frac{(4n+6)}{\ln(4n+5)}$ and $\frac{(4n+6)}{\ln(2n^2+8n+7)}$ be minimum. Fig. 4(a) indicates that the least number of IGBTs based on both the algorithms are given for $n = 1$.

B. Minimizing the Number of Sources for Constant Levels

The main goal of this section is determining the value of n to minimize the number of sources for constant number of sources. From (12), (25), and (28), it is obvious that

$$N_{\mathrm{source}} = \ln(N_{\mathrm{level,FA}}) \times \frac{(2n+2)}{\ln(4n+5)} \tag{45}$$

$$N_{\mathrm{source}} = \ln(N_{\mathrm{level,SA}}) \times \frac{(2n+2)}{\ln(2n^2+8n+7)}. \tag{46}$$

Variation of $\frac{(2n+2)}{\ln(4n+5)}$ and $\frac{(2n+2)}{\ln(2n^2+8n+7)}$ against n is shown in Fig. 4(b). It is clear that $n = 1$ gives the optimal structure for both the proposed first and second algorithms.

C. Minimizing the Number of Drivers for Constant Levels

Optimization of the proposed cascade topology to produce constant number of levels with minimum number drivers is analyzed in this section. By the use of (12), (25), and (27), N_{driver} based on both algorithms are computed as follows:

$$N_{\mathrm{driver}} = \ln(N_{\mathrm{level,FA}}) \times \frac{(2n+6)}{\ln(4n+5)} \tag{47}$$

$$N_{\mathrm{driver}} = \ln(N_{\mathrm{level,SA}}) \times \frac{(2n+6)}{\ln(2n^2+8n+7)}. \tag{48}$$

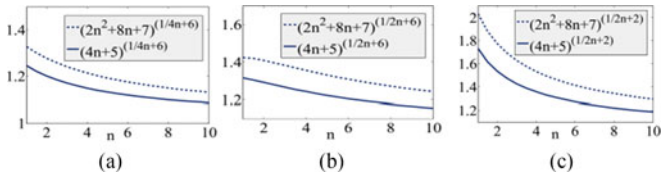

Fig. 5. Related curves to optimize the proposed cascade structure in terms of maximizing the number of levels for constant number of (a) IGBTs, (b) dc sources, (c) drivers to obtain parameter *n*.

N_{driver} is minimized when $\frac{(2n+6)}{\ln(4n+5)}$ and $\frac{(2n+6)}{\ln(2n^2+8n+7)}$ be minimum. Fig. 4(c) shows that $n = 1$ gives the optimal circuit.

D. Minimizing Voltage Rating on Switches for Constant Levels

Optimal structure to withstand the minimum value of voltage rating on switches of the proposed CSLMI structure with constant number of levels is determined in this section. Considering (42), TMVR_{sw} is minimized when $2 + \frac{G}{2(n+1)}$ be minimum. Fig. 4(d) indicates that the least value of the total voltage rating on switches is given for $n = 1$.

E. Maximizing N_{level} for Constant Number of IGBTs

In this section, the aim is maximizing the number of generated levels for constant number of IGBTs. Based on (12), (25), and (26), we have

$$N_{\text{level,FA}} = \left[(4n+5)^{1/(4n+6)}\right]^{N_{\text{IGBT}}} \tag{49}$$

$$N_{\text{level,SA}} = \left[(2n^2+8n+7)^{1/(4n+6)}\right]^{N_{\text{IGBT}}}. \tag{50}$$

To maximize $N_{\text{level,FA}}$ and $N_{\text{level,SA}}$, it is necessary that the equations $(4n+5)^{1/(4n+6)}$ and $(2n^2+8n+7)^{1/(4n+6)}$ be maximum, respectively. Fig. 5(a) shows the variation of $(4n+5)^{1/(4n+6)}$ and $(2n^2+8n+7)^{1/(4n+6)}$ versus *n*. This figure indicates that $n = 1$ gives maximum levels for both algorithms.

F. Maximizing N_{level} for Constant Number of Drivers

Obtaining the optimal value for *n* to maximize the number of levels for constant number of IGBTs is the main goal of this section. Considering (12), (25), and (27), we have

$$N_{\text{level,FA}} = \left[(4n+5)^{1/(2n+6)}\right]^{N_{\text{driver}}} \tag{51}$$

$$N_{\text{level,SA}} = \left[(2n^2+8n+7)^{1/(2n+6)}\right]^{N_{\text{driver}}}. \tag{52}$$

$N_{\text{level,FA}}$ and $N_{\text{level,SA}}$ are maximized when $(4n+5)^{1/(2n+6)}$ and $(2n^2+8n+7)^{1/(2n+6)}$ are maximum, respectively. The variation of $(4n+5)^{1/(2n+6)}$ and $(2n^2+8n+7)^{1/(2n+6)}$ against *n* are indicated in Fig. 5(b). According to this figure, it can be seen that $n = 1$ presents the optimal topology.

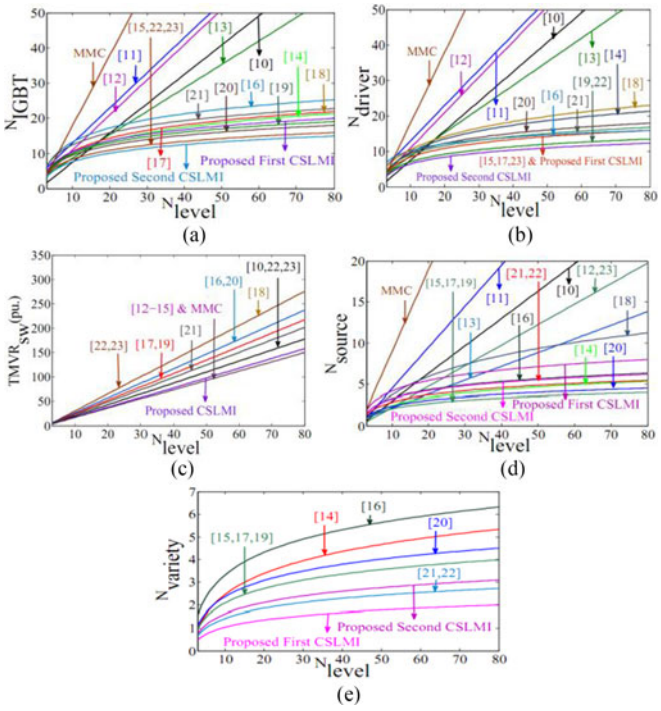

Fig. 6. Comparison of (a) N_{IGBTs}, (b) N_{driver}, (c) maximum voltage rating on switches, (d) N_{sources},(e) N_{variety} in various topologies.

G. Maximizing N_{level} for Constant Number of DC Sources

In this section, optimal topology to maximize the number of produced levels for constant number of dc sources is obtained. Based on (12), (25), and (28), we have

$$N_{\text{level,FA}} = \left[(4n+5)^{1/(2n+2)}\right]^{N_{\text{source}}} \tag{53}$$

$$N_{\text{level,SA}} = \left[(2n^2+8n+7)^{1/(2n+2)}\right]^{N_{\text{source}}}. \tag{54}$$

Fig. 5(c) indicates the variation of $(4n+5)^{1/(2n+2)}$ and $(2n^2+8n+7)^{1/(2n+2)}$ against *n*. This figure shows that $n = 1$ gives the optimal topology.

VI. Comparison of the Proposed Cascade Topology With Other Recommended Topologies in [10]–[23]

To show the merits of the recommended CSLMI, the proposed topology based on the two algorithms is compared with other topologies in [10]–[23] and modular multilevel inverter (MMC). CHB with the proposed four algorithms for determination of dc sources values in [12]–[15] has been considered for comparison. For presented topologies in [17], [18], [20], the best algorithm is considered for comparison. Fig. 6(a) compares the number of IGBTs in various structures. This figure proves that the proposed topology based on the second algorithm requires lower IGBTs compared to [10]–[23] and MMC. The number of drivers against levels in different structures is indicated in Fig. 6(b). This figure shows that the recommended structure based on the second algorithm requires lower drivers. The variation of the normalized

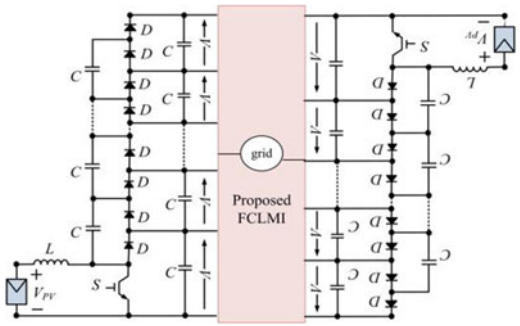

Fig. 7. Proposed system for application of FCLMI in PV panels using the presented one-input multioutput dc–dc converter in [26].

maximum voltage rating on switches versus the number of levels for different structures is indicated in Fig. 6(c). This comparison indicates that this criterion in the proposed topology is less than [10], [11], [16]–[23], and the MMC structure. The number of dc sources in various topologies is shown in Fig. 6(d). According to this figure, the proposed topology based on the second algorithm needs less number of sources than [10]–[13], [23], and MMC. However, the proposed second algorithm requires almost two dc sources more than [14], [15], [17], [19]–[22]. The number of various voltage amplitudes of the used sources (N_{variety}) in various cascaded topologies is indicated in Fig. 6(e). Based on this figure, the proposed CSLMI based on two algorithms has lower number of various voltage amplitudes of the used sources. The variety of the magnitudes of sources is an important factor in determining the cost of the inverters. The proposed topology is used in photovoltaic (PV) panels. For these applications, using several FSLMIs is impossible because the voltage generated by PV is limited and the variety of the amount of input sources for the proposed cascade topology does not allow for using it in PV applications. For this aim, only one FSLMI is used, wherein their input sources can be replaced with PV panels. Also, one-input multioutput dc–dc converters can be used for this aim. For instance, the proposed one-input multioutput dc–dc inverter in [26] can be used for the proposed FSLMI, which is shown in Fig. 7. By controlling the duty cycle of the both switches in the one-input multioutput dc–dc converters, the voltage on all output capacitors are adjusted to the same voltages. In high-voltage induction motor drives, lower THD is needed.

VII. Power Loss Evaluation

There are two types of power losses in the presented topology which are called conduction and switching losses. Conduction losses (P_c) occur when the switch conducts the current. P_c is the sum of conduction losses in IGBT $(P_{c,\text{IGBT}})$ and anti-parallel diode $(P_{c,D})$. $P_{c,\text{IGBT}}$ and $P_{c,D}$ are

$$P_{c,\text{IGBT}} = z(t) \cdot \left[\frac{1}{2\pi}\int_0^{2\pi} V_{\text{on,IGBT}} I + R_{\text{on,IGBT}} I^{\beta+1} d(wt)\right] \tag{55}$$

$$P_{c,D} = w(t) \cdot \left[\frac{1}{2\pi}\int_0^{2\pi} V_{\text{on},D} I + R_{\text{on},D} I^{2} d(wt)\right]. \tag{56}$$

In the above equations, $V_{\text{on,IGBT}}$ and $V_{\text{on},D}$ are the on-state voltage drop of the IGBT and antiparallel diode, respectively. Also, $R_{\text{on,IGBT}}$ and $R_{\text{on},D}$ are the on-state resistance of the IGBT and antiparallel diode, respectively. Moreover, *z(t)* and *w(t)* are the number of on-state IGBTs and antiparallel diodes in current path. The conducted current by semiconductor is assumed to be almost sinusoidal ($I = I_p \sin(wt)$). β is a constant factor which depends on the specification of the IGBT. The switching loss (P_{sw}) is the power losses during the turn-ON $(P_{\text{sw,on}})$ and the turn-OFF $(P_{\text{sw,off}})$ switching of the switch which are obtained as follows:

$$P_{\text{sw,on}} = \frac{N_{\text{on}}}{T}\int_0^{t_{\text{on}}} V(t)\cdot I(t)dt = \frac{V_{\text{sw}}\cdot I\cdot t_{\text{on}}\cdot N_{\text{on}}}{6T} \tag{57}$$

$$P_{\text{sw,off}} = \frac{N_{\text{off}}}{T}\int_0^{t_{\text{off}}} V(t)\cdot I(t)dt = \frac{V_{\text{sw}}\cdot I\cdot t_{\text{off}}\cdot N_{\text{off}}}{6T} \tag{58}$$

where N_{on} and N_{off} are the number of turning ON and OFF switches during a fundamental cycle (1/*T*). In addition, t_{on} and t_{off} are the turning ON and OFF time of switches. Also, V_{sw} is the maximum voltage on switches. Therefore, considering (55)–(58), the power losses of the proposed converter (P_{loss}) will be

$$P_{\text{loss}} = P_{c,\text{IGBT}} + P_{c,D} + P_{\text{sw,on}} + P_{\text{sw,off}}. \tag{59}$$

VIII. Experimental Works

In order to prove the ability of proposed structures, the experimental results for a 31-level fundamental topology based on the second algorithm and an 81-level cascade inverter based on the first algorithm are presented. Several switching techniques can be used for multilevel inverters such as sinusoidal PWM method, space vector PWM, and fundamental frequency switching method [27], [28]. Fundamental frequency switching method is utilized to generate the pulses of switches. The Fourier series of the output voltage waveform (V_o) with N_{level} and equal amplitudes can be written as follows:

$$V_o(t) = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_{\text{dc}}}{n\pi}\cos(n\theta_j)\sin(\text{nwt}),$$
$$\text{for}\quad j = 1, \ldots, N_{\text{level}} \tag{60}$$

where θ_j are switching angles and are calculated by

$$\theta_j = \sin^{-1}\left(\frac{2j-1}{N_{\text{level}}}\right), \quad \text{for} \quad j = 1, \ldots, N_{\text{level}}. \tag{61}$$

The THD of the output voltage waveform is [19], [20]

$$\text{THD} = \frac{\sqrt{\sum_{h=3,5,\ldots}^{\infty} {V_h}^2}}{V_1} = \sqrt{\left(\frac{V_o}{V_1}\right)^2 - 1} \tag{62}$$

where V_h, V_o, and V_1 are the RMS values of *h* order component, $V_o(t)$, and the fundamental of the output voltage, respectively.

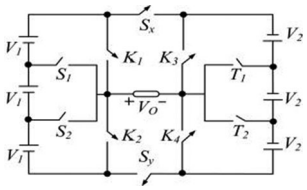

Fig. 8. Experimented fundamental 31-level inverter topology based on the illustrated second algorithm.

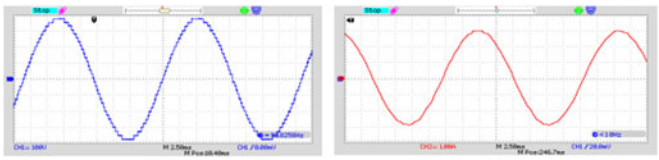

Fig. 9. Experimental waveforms of 31-level inverter: (a) output voltage, (b) the zoomed output voltage waveform, and (c) output current.

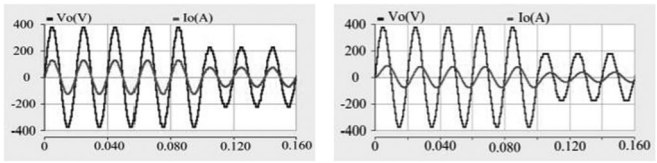

Fig. 10. Output voltage and current waveforms considering variations of amplitude modulation and load: (a) $M_a = 0.612$, $R = 30$, $L = 0$ mH and (b) $M_a = 0.5$, $R = 30$, $L = 120$ mH.

V_o and V_1 are calculated as follows [19], [20]:

$$V_o = \frac{2\sqrt{2}V_{dc}}{\pi}\sqrt{\sum_{n=1,3,5,\ldots}^{\infty}\left(\sum_{j=1}^{N_{level}}\frac{\cos(n\theta_j)}{n}\right)^2} \tag{63}$$

$$V_1 = \frac{2\sqrt{2}V_{dc}}{\pi}\sum_{j=1}^{N_{level}}\cos(\theta_j). \tag{64}$$

A. Experimented 31-Level Converter

The circuit of the 31-level inverter based on the second algorithm is shown in Fig. 8. The values of dc sources are $V_1 = 25$ V and $V_2 = 100$ V. The value of output voltage frequency is 50 Hz. The R–L load with the values of $R = 130\ \Omega$ and $L = 55$ mH is used for this topology. The output voltage waveform of 31-level inverter is indicated in Fig. 9(a). It is clear that the maximum output voltage is 375 V. According to this figure, the levels are 0, ± 25 V, ± 50 V, $\ldots$, ± 350 V, ± 375 V. Fig. 9(b) shows the output current of the 31-level inverter. In order to show the robustness of the proposed converter for working at different modulation indexes and loads, the studied 31-level inverter is analyzed based on these criterions. It is noticeable that the variations is happened at $t = 0.1$ s. Fig. 10(a) indicates the output voltage and current waveforms, simultaneously. In this figure, the values of R–L load is selected as $R = 30\ \Omega$ and $L = 0$ mH. In fact, the load

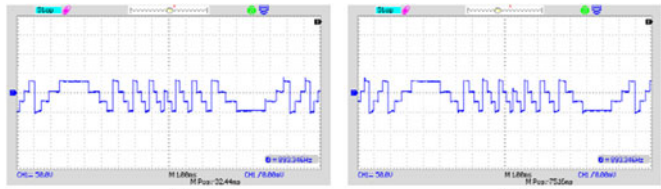

Fig. 11. Voltage waveforms of bidirectional switches in the 31-level inverter: (a) S_1 and (b) S_2.

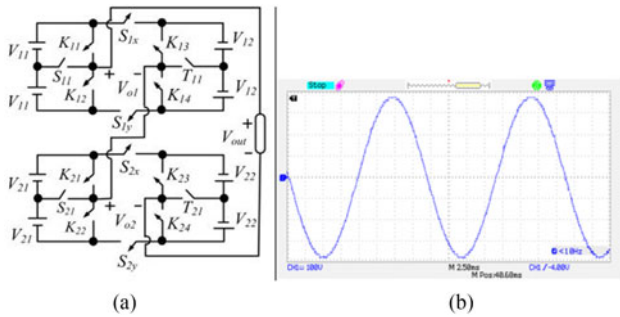

Fig. 12. (a) Proposed 81-level cascade inverter base on described first algorithm and (b) output voltage of cascade inverter (V_{out}).

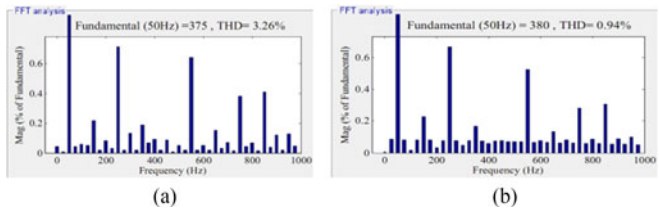

Fig. 13. (a) Frequency spectrum of the 31-level inverter (THD = 3.26%). (b) Frequency spectrum of the 81-level inverter (THD = 0.94%).

is resistive which causes the value of the output power factor to be one. As shown in this figure, the amplitude modulation (M_a) is changed from 1 to 0.612 at $t = 0.1$ s. It causes the number of generated levels to change from 31 to 19. Fig. 10(b) shows the output voltage and current waveforms for $R = 30\ \Omega$ and $L = 120$ mH. In this figure, the value of M_a is changed from 1 to 0.5 at $t = 0.1$ s, which causes the number of levels to be varied from 31 to 15 at $t = 0.1$ s. All changes shown in Fig. 10 indicate that the proposed topology can be used in different amplitudes of modulations and loads. Fig. 11 indicates the voltage waveforms of bidirectional switches in the 31-level inverter. It shows that the maximum voltage on switches S_1 and S_2 is 50 V.

B. Experimented 81-Level Converter

The structure of 81-level cascade inverter based on the proposed first method is indicated in Fig. 12(a). For this structure, $R = 250\ \Omega$ and $L = 45$ mH is used. Also, the values of sources based on the proposed first algorithm are $V_{11} = V_{12} = 9.5$ V, $V_{21} = V_{22} = 85.5$ V. The experimented output voltage waveform of the 81-level cascade structure inverter (V_{out}) is indicated in Fig. 12(b). The values of levels at output voltage

of the cascade inverter are 0, ±9.5 V, ±19 V, . . ., ±370.5 V, ±380 V. The frequency spectrums for the output voltage of 31-level and 81-level topologies are shown in Fig. 13(a) and (b), respectively. Based on these figures, THDs of the 31-level and 81-level topologies are 3.26% and 0.94%, respectively.

IX. Conclusion

A new switch-ladder cascade topology for multilevel inverter was described in this paper. The presented cascade topology was optimized due to the extended feature of proposed topology. The main aim of optimization was generating maximum number of output voltage levels with minimum number of power electronic components and voltage rating on switches. The result of optimization indicated that $n = 1$ can satisfy all required aims. The optimum structure was compared with the recommended structures in [10]–[23] and MMC in terms of power electronic components and voltage rating on switches. The results of comparison indicated that the proposed cascade topology could overcome the disadvantages of other structures.

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