

Application of Transformer-less UPFC for Interconnecting Synchronous AC Grids

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Abstract—A transformer-less UPFC based on an innovative configuration of two cascaded multilevel inverters (CMIs) has been proposed recently, which is suitable for power flow control between two interconnected synchronous AC grids. The active power as well as the reactive power can be independently controlled by the new transformer-less UPFC. In addition, the semiconductor device ratings (SDPRs) for different power flow control solutions have been investigated. It can be found that cascade multilevel inverter based transformer-less UPFC has much lower SDPR when compared to MMLC based back-to-back HVDC system, indicating significant cost saving when use transformer-less UPFC for power flow control. Experimental results based on 13.8 kV/ 2MVA transformers-less UPFC prototype are shown to validate the theoretical analysis.

Keywords— Cascade Multilevel Inverter (CMI), UPFC, HVDC, MMLC

I. INTRODUCTION

The North American power grid is a complicated mesh structure. These meshed networks are over-crowded and are often subject to severe congestions. One typical example is the Michigan Upper Peninsula (UP) grid scenario as shown in Fig. 1 [1]. The Power demand is high on south and east side of Lake Michigan. Most of the power flow follows the low impedance path south of Lake Michigan; however, a small, but significant, portion of power finds its way through high impedance path in the UP. Due to this loop flow problems, Eastern UP grid is “split” from that of West UP in order to prevent overloading of lines/equipment and to eliminate under voltage. UP split is necessary for 95% time of a year. As a result, it’s difficult to perform scheduled maintenance, to regulate voltage in eastern UP. To solve this problem, the East UP is going to connect to Lower Peninsula (LP) through the voltage source converters (VSC) back to back high voltage direct current (HVDC) system [1].

Traditionally, HVDC transmission system have been used for long distance power transmission and interconnecting asynchronous grids. Recently, VSC based back to back HVDC system was also applied to interconnect synchronous grids for power flow control [1], [2]. VSC based back to back HVDC system has additional benefits, such as the ability to black-start and the ability to use either converters to function as STATCOMs in an islanded case [1]. However, the main drawback of the back to back HVDC system is the

requirement of two full-power rating converters to interface two grids, which significantly reduces the system efficiency and increases the cost.

Recently, a cascade multilevel inverter (CMI) based modular transformer-less unified power flow controller (UPFC) has been proposed [3], which has several advantages, such as complete transformer-less, light weight, high efficiency, high reliability, low cost, and fast dynamic response. In this paper, the transformer-less UPFC is applied to interconnect two synchronous AC grids for independent active/reactive power control. First, a comparison of the total semiconductor device power ratings (SDPR) between different power flow solutions (mainly back to back HVDC and transformer-less UPFC) is analyzed. The analytic results will show that the SDPR of transformer-less UPFC could be 8 times smaller than the back to back HVDC system when used for power flow control. The corresponding system configuration, power flow and dc-link voltage control of transformer-less UPFC will be introduced and experimentally verified at 13.8 kV/ 2MVA test setup.

II. OPERATION PRINCIPLE OF THE TRANSFORMER-LESS UPFC

Fig. 2 shows the configuration of the new transformer-less UPFC. As shown in Fig. 2 (a), the transformer-less UPFC consists of two cascade multilevel inverters (CMIs), one is series CMI, which is directly connected in series with the transmission line; while the other is shunt CMI, which is connected in parallel to the sending end after series CMI. Each CMI is composed of a series of cascaded H-bridge modules as shown in Fig. 2 (b) [3].

Fig. 3 shows the phasor diagram for the transformer-less UPFC, where \vec{V}_{s0} and \vec{V}_R are the original sending-end and receiving-end voltage, respectively. Here, \vec{V}_{s0} is aligned with real axis, which means phase angle of \vec{V}_{s0} is zero. The series CMI is controlled to generate a desired voltage \vec{V}_C for obtaining the new sending-end voltage \vec{V}_S , which in turn, controls active and reactive power flows through the transmission line. Meanwhile, the shunt CMI injects a current \vec{I}_P to the new sending-end bus to make zero active power into

both CMIs, i.e., to make the series CMI current \vec{I}_C and the shunt CMI current \vec{I}_P be perpendicular to their voltages \vec{V}_C and \vec{V}_S , respectively. As a result, both series and shunt CMIs only need to provide the reactive power. In such a way, it is possible to apply the CMIs to the transformer-less UPFC with floating dc capacitors for H-bridge modules.

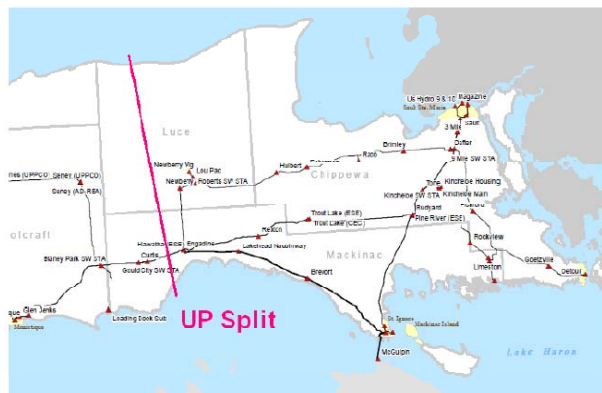
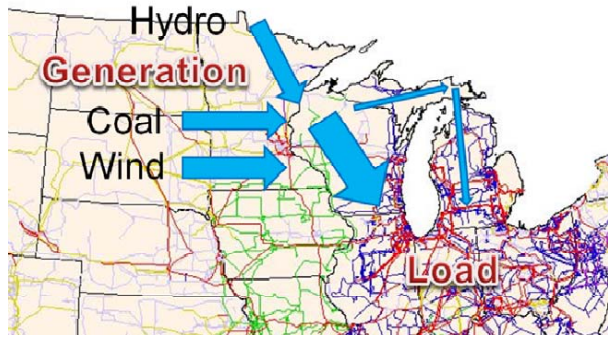


Fig. 1. Michigan UP grid scenario, (a) Illustration of power flow in Upper Midwestern US, and (b) Eastern UP transmission system with split

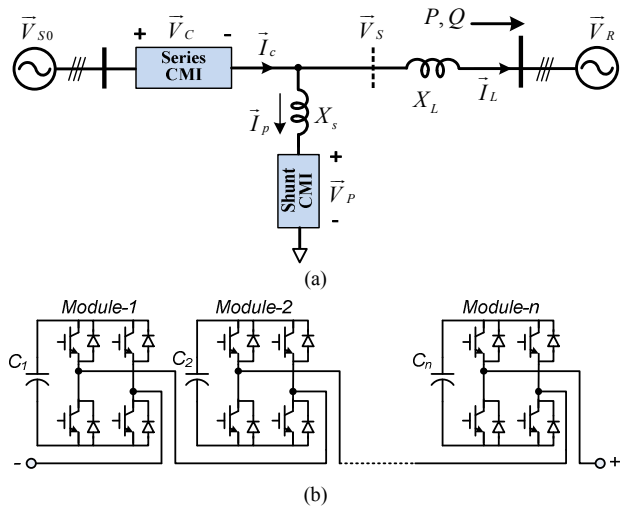


Fig. 2. New transformer-less UPFC, (a) System configuration, (b) One phase of the cascaded multilevel inverter.

For the system without UPFC compensation (or $\vec{V}_C = 0$) the original active power P_0 and reactive power Q_0 are decided as

$$P_0 = \frac{V_{S0}V_R}{X_L} \sin \delta_0, \quad Q_0 = \frac{V_{S0}V_R \cos \delta_0 - V_R^2}{X_L}. \quad (1)$$

It indicates that the power flow is decided by the parameters of voltage amplitude V_{S0} and V_R , line impedance X_L and phase angle difference δ_0 between sending-end voltage and receiving-end voltage. In general, the active power is more related to phase angle and the reactive power is more related to the voltage amplitude.

When UPFC is applied for interconnecting synchronous AC grids, two different scenarios are considered:

- 1) UPFC applied to increase the power flow: the original phase angle difference δ_0 between \vec{V}_{S0} and \vec{V}_R is small. Power/current flow can be controlled to a higher value when the phase angle different is controlled from δ_0 to δ_s by UPFC. The corresponding phasor diagram is shown in Fig. 3 (a).
- 2) UPFC applied to decrease the power flow: In this case, the original phase angle difference δ_0 between \vec{V}_{S0} and \vec{V}_R is big, e.g. 30° . Therefore, it is impossible to close this line directly; otherwise, hug current/power will go through the line to cause the overload. Here, series voltage \vec{V}_C is injected to adjust the phase angle δ_0 to δ_s with a smaller value, the power flow through the line then is controlled to a limited value. The corresponding phasor diagram is shown in Fig. 3 (b).

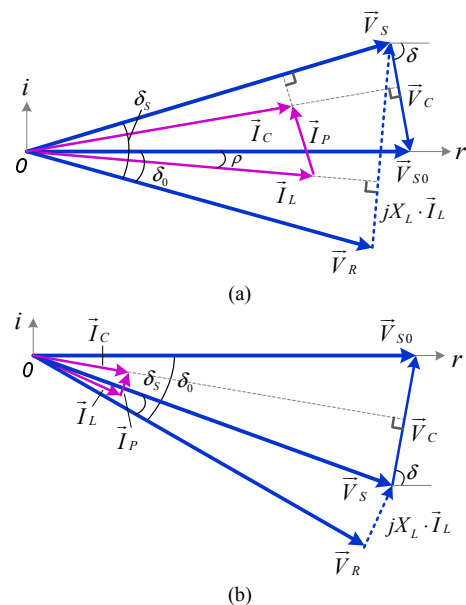


Fig. 3. Illustration of UPFC power flow regulation, (a) UPFC applied to increase the power flow and (b) UPFC applied to decrease the power flow.

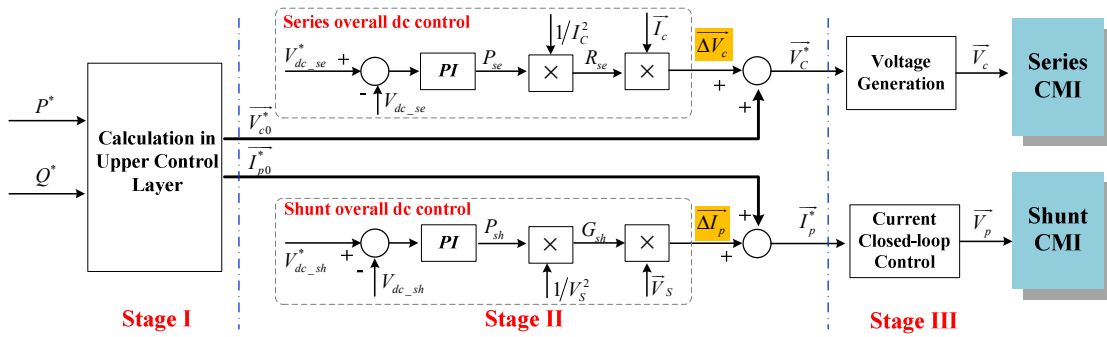


Fig. 4. Overall control diagram of the transformer-less UPFC.

It is desired to design a control system, which can independently regulate the active power P and reactive Q in the line, at the same time, maintain the capacitor voltages of both CMIs at the given value. Fig. 4 shows the overall control system, which is divided into three stages, i.e. stage I to stage III [9].

Stage I: the calculation from P^*/Q^* to \bar{V}_{C0}^* and \bar{I}_{p0}^* . As mentioned before, the \bar{V}_{C0}^* is the voltage reference for series CMI, which is generated according to the transmission line power command, while \bar{I}_{p0}^* is current reference for shunt CMI, which is used to keep zero active power for both CMIs.

Stage II: overall dc-link voltage regulation. In order to control dc-link voltage with better robustness, two variables $\overline{\Delta V_C}$ and $\overline{\Delta I_p}$ were introduced for the independent dc-link voltage regulation of series CMI and shunt CMI, respectively, as shown in Fig. 4 (a). In this figure, $V_{dc_sh}^*$ and $V_{dc_se}^*$ are dc voltage references for shunt and series CMIs, respectively; V_{dc_sh} and V_{dc_se} are the averaged dc feedback of shunt and series CMIs, respectively. For the series CMI, P_{se} is the output of overall dc-link voltage regulation loop, R_{se} is then calculated by dividing P_{se} by I_c^2 (square of *rms* value of series CMI current), finally $\overline{\Delta V_C}$ is the product of R_{se} and series CMI current \bar{I}_c . Obviously, the introduced $\overline{\Delta V_C}$ is always in phase with series CMI \bar{I}_c , which can be regarded as *active-voltage* component. Basically, R_{se} is the equivalent resistance of series CMI, and the dc-link can be balanced when P_{se} is equal to P_{loss} (total power loss of series CMI). For the shunt CMI, $\overline{\Delta I_p}$ is introduced for the dc-link voltage control in a similar way.

Stage III: voltage and current generation for series and shunt CMI, respectively. For series CMI, output voltage could be directly generated from the reference \bar{V}_C^* by fundamental frequency modulation (FFM). While for shunt CMI, decoupling feedback current control is used to control output

current to follow the reference current \bar{I}_p^* , as shown in Fig. 4 (c). The transformer-less UPFC modulation and control method has been introduced in [9] in detail.

III. SSDPR COMPARISON BETWEEN BACK TO BACK HVDC SYSTEM AND TRANSFORMER-LESS UPFC SYSTEM

Semiconductor Device Power Rating (SDPR) is an indication of how much total silicon area is needed for the semiconductor devices, which is one of the most important indicators to estimate the inverter/converter cost. The individual device power rating is defined as the product of voltage and current stress of the semiconductor device, the inverter/converter SDPR is the summation of individual device power rating [4], [5]:

$$SDPR = \sum_{k=1}^n V_k I_k, \quad (1)$$

where n is the total number of semiconductor devices in the inverter/converter, and V_k, I_k are the voltage and current stress of the k^{th} semiconductor device (e.g. IGBTs) respectively. The overall system SDPR (SSDPR) is then decided by

$$SSDPR = SDPR * \eta, \quad (2)$$

where η represents the inverter/converter rating with respect to system rating. For instance, the MVA rating of a series Flexible AC Transmission System (FACTS) device will often be a small fraction of the throughput line MVA, considering the per unit line impedance is usually a small fraction of the line [5]-[7].

A. SDPR of the Basic Three-phase Converter

Fig. 5 (a) shows the topology of basic three-phase inverter/rectifier. The current stress of the IGBT is $\sqrt{2}I_g$, where I_g is the *rms* value of output current. The voltage stress is equal to the dc-link voltage, and its minimum value is $\sqrt{2}V_g$ when SVPWM or SPWM with 3rd harmonic injection is used with maximum modulation index, where the V_g is the *rms* value of line-to-line grid voltage. Therefore, the overall SDPR for all 6 IGBTs is

$$SDPR = 6 \cdot \sqrt{2}I_g \cdot \sqrt{2}V_g = 12V_g I_g. \quad (3)$$

In all analysis, the line to line AC voltage and line currents are considered as the base values. Hence, the SDPR for a three phase inverter or rectifier is

$$SDPR = 12 pu . \quad (4)$$

Hence, the SDPR for a three phase inverter/rectifier is 12 pu when the power exchange between inverter and AC grid is equal to 1 pu.

B. SDPR of Half-bridge MMLC

Fig. 5 (b) shows the topology of half-bridge based modular multilevel converters (MMLC), which is the most popular VSC topology for HVDC system [8]. Here, V_g is the line-to-line AC voltage, i_{arm} is the current through the upper arm, i_{DC} is the current through the DC link, and i_g is the current through AC grid. Comparing the basic cell (half bridge) of the MMLC to the basic cell (a single switch) of the basic three-phase converter shown in Fig. 5 (a), it can be observed that the number of IGBTs in the basic cell is doubled. Similarly, the minimum dc voltage for a given AC voltage is $\sqrt{2}V_g$, which is essentially the voltage stress of the switches.

According to the current and voltage derivations in [8], the current through each arm of the MMLC circuit is given as

$$i_{arm} = i_g / 2 + i_{dc} / 3 . \quad (5)$$

Considering unity power factor and the power balance between dc side and ac side, we have

$$P = \sqrt{3}V_g I_g = V_{dc} I_{dc} . \quad (6)$$

where $V_{dc} = \sqrt{2}V_g$. Then we can derive the arm current from (5) and (6) as

$$i_{arm} = \left(\frac{1}{2} + \frac{1}{\sqrt{6}} \right) I_g . \quad (7)$$

The arm current $i_{arm} \approx i_g$ with consideration of circulating current. As a result, the current stress of each of the IGBTs is considered as $\sqrt{2}I_g$. Therefore, the overall SDPR for all 12 IGBTs is

$$SDPR = 12 \cdot \sqrt{2}I_g \cdot \sqrt{2}V_g = 24 pu . \quad (8)$$

It is notable that the SDPR of Half-bridge MMLC is independent of the number of modules. For instance, if the number of half-bridge modules in each arm is doubled, the overall SDPR still remains the same.

C. SDPR of the Cascade Multilevel Converter

Fig. 5 (c) shows the topology of cascaded multilevel inverter (CMI). Compared to the topology of basic three-phase converter shown in Fig. 5 (a), the number of IGBTs of CMI is doubled, and each IGBT has same current rating but half of the voltage rating.

$$SDPR = 12 \cdot \sqrt{2}I_g \cdot \frac{\sqrt{2}V_g}{2} = 12 pu . \quad (9)$$

It should be noted again that the SDPR for CMI is independent of number of H-bridge modules. Increasing the number of H-bridge modules for CMI doesn't help to reduce the SDPR.

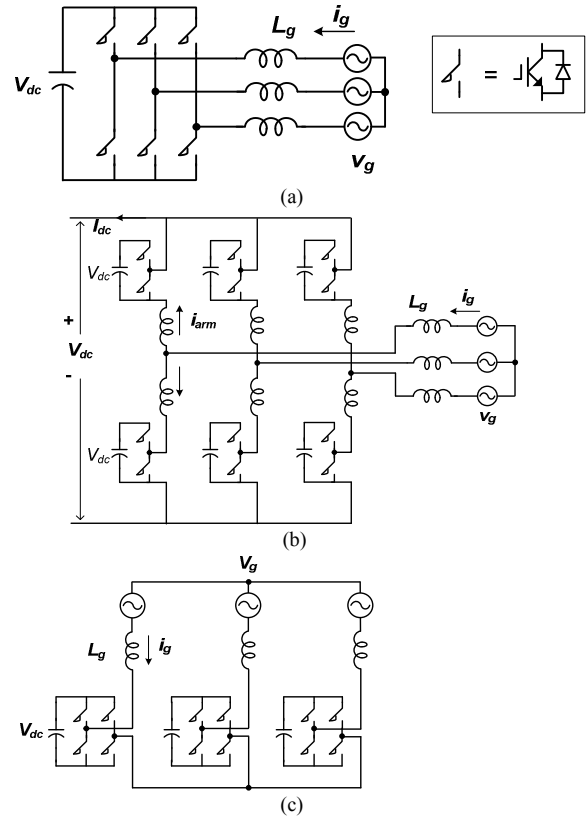


Fig. 5. Different inverter/converter topologies, (a) basic three-phase inverter/rectifier, (b) half-bridge MMLC, and (c) cascade multilevel inverter (CMI).

D. SSDPR Comparison between Back to Back HVDC System and Transformer-less UPFC System

In order to perform power flow control, two MMLC converters as shown in Fig. 5 (b) have to be connected in a back-to-back manner. Therefore, the SSDPR for the back-to-back MMLC based HVDC system is

$$SSDPR_{HVDC} = 2 \cdot 24 pu = 48 pu . \quad (10)$$

For a UPFC based Power flow control system, considering 30° phase angle difference between two synchronous grids \vec{V}_{s0} and \vec{V}_R , the total UPFC rating is 1 pu as analyzed in [3], [9], therefore, the SDPR for a transformer-less UPFC is calculated as

$$SSDPR_{UPFC} = 1 \cdot 12 pu = 12 pu , \quad (11)$$

which is less than 1/4 of back-to-back HVDC system. It should be noted that the transformer-less UPFC can also control power flow without shunt CMI, in this case, UPFC operates just like the Static Synchronous Series Compensator (SSSC). The system rating is 0.5 pu without shunt CMI, and the overall SDPR becomes $0.5 \times 12 = 6 pu$, which is 8 times

smaller than that of back-to-back HVDC system. In summary, the cascade multilevel inverter based transformer-less UPFC has much lower SDPR when compared to MMLC based back-to-back HVDC system, indicating significant cost saving when used for power flow control.

IV. EXPERIMENTAL RESULTS

A 13.8-kV/ 2-MVA transformers-less UPFC prototype has been developed to validate the UPFC power flow control functionality. The test setup is shown in Fig. 6, and the main system parameter for the prototype is given in TABLE I. In Fig. 6, the sending-end voltage \vec{V}_{S0} has the same amplitude as receiving-end voltage \vec{V}_R (13.8 kV), but 30° phase leading. This 30° phase leading is introduced by the Y/ Δ transformer. As mentioned before, it is impossible to directly close this line without UPFC compensation, otherwise huge current/power will flow through the line due to the 30-degree voltage difference. When the new transformer-less UPFC is applied to interconnect these two grids, it provides complete flexibility and controllability, which means the current/power can be controlled to any desired value.

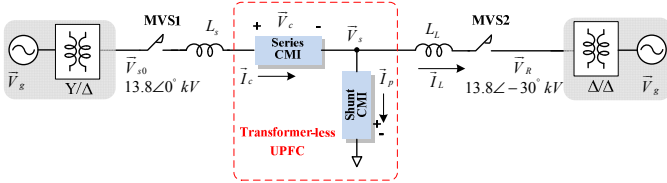


Fig. 6. The system configuration for 13.8-kV/ 2-MVA UPFC test setup.

TABLE I. System Parameters of the Transformer-less UPFC Test Setup

Parameters	Value
Rated power	2 MVA
V_{S0} (Phase-phase rms)	13.8 kV $\angle 0^\circ$, 60 Hz
V_R (Phase-phase rms)	13.8 kV $\angle -30^\circ$, 60 Hz
Equivalent line inductance L_S	0.12 pu
Equivalent line inductance L_L	0.36 pu
Series CMI per phase	8 H-bridge modules
Shunt CMI per phase	20 H-bridge modules
Nominal Series CMI V_{dc}	450V~600V
Nominal Shunt CMI V_{dc}	550V
DC capacitance of each CMI	2350 μ F

A UPFC can simply control the magnitude and phase angle of the injected voltage in real time so as to regulate the active and reactive power flow in the line to satisfy load demand and system operating conditions. It is notable that the UPFC is able to control, simultaneously or selectively, all the parameters affecting power flow in the transmission line (i.e., voltage magnitude, impedance, and phase angle). Here the series CMI is used as impedance compensator, while the shunt CMI is used as reactive power compensator. The shunt CMI will compensate the line reactive power and to make sure the reactive power for both side grids are the same. Therefore, the

injected series CMI voltage \vec{V}_C and the shunt CMI current \vec{I}_P references are calculated as follows:

- 1) δ_S is decided firstly according to the system power command;
- 2) \vec{V}_C is assumed in phase with \vec{V}_{LS} , of course the following equation holds: $\vec{V}_{S0} = \vec{V}_S + \vec{V}_C + \vec{V}_{LS}$;
- 3) The amplitude of \vec{V}_S is then decided to guarantee the phase angle of \vec{V}_C (or \vec{V}_{LS}) leads \vec{V}_S by 105° . In such a case, it can be proven that the phase angle of \vec{V}_{LL} would lead \vec{V}_S by 75° . Since the currents of \vec{I}_C and \vec{I}_L lag their voltages by 90° , the phase angle of \vec{I}_C would lead \vec{V}_S by 15° , while the phase angle of \vec{I}_L would lag \vec{V}_S by 15° .
- 4) The shunt current will be chosen to guarantee current amplitude of \vec{I}_C is equao to that of \vec{I}_L , as a result, the shunt current \vec{I}_P would be perpendicular with \vec{V}_S .

Fig. 7 shows the phasor diagram for different operating points of UPFC power flow control, two cases are shown here: (a) Case A: $\delta_S = 22^\circ$ and (b) Case B: $\delta_S = 7^\circ$.

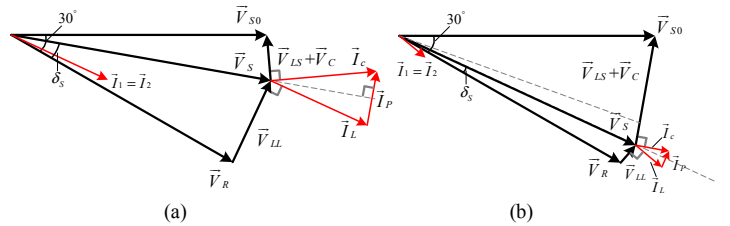
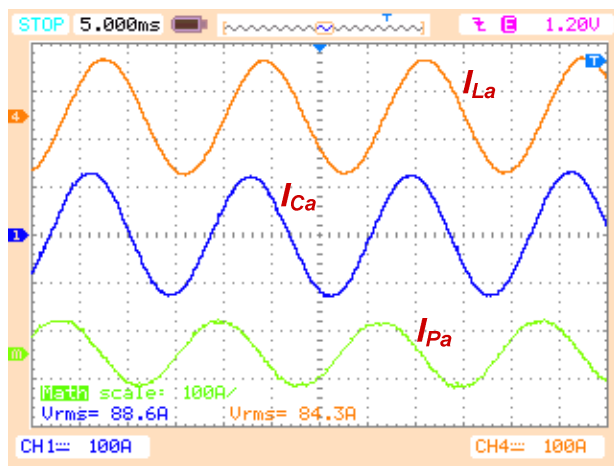


Fig. 7. Phasor diagram for different operating points of UPFC power flow control, (a) Case A: $\delta_S = 22^\circ$ and (b) Case B: $\delta_S = 7^\circ$.

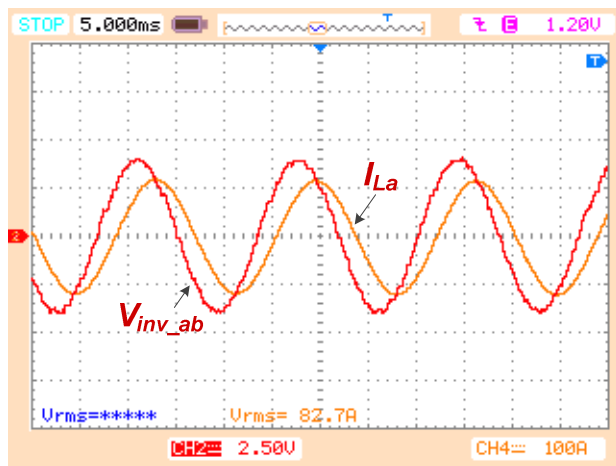
Fig. 8 shows the experimental waveform of transformer-less UPFC operated at Case A: $\delta_S = 22^\circ$: (a) transmission line current I_{La} , sending-end current I_{Ca} and shunt current I_{pa} , and (b) $V_{inv,ab}$ and I_{La} , where the $V_{inv,ab}$ is the voltage of series CMI output voltage $V_{C,ab}$ plus shunt CMI output voltage $V_{P,ab}$. The displayed line voltage $V_{inv,ab}$ is the voltage measured at the secondary of the potential transformer (PT) with turn ratio is $120 \times 41 : 1$. In this case, due to the large value of power angle δ_S , the corresponding line current $I_L = 84$ A, active power $P = 1.8$ MW, and reactive power $Q = 0.6$ MVar. In addition, Fig. 9 shows averaged dc link voltage for both series and shunt CMIs, where the dc voltage reference for series CMI is 450 V and voltage reference for shunt CMI is 550 V. The dc voltage references are chosen to keep the modulation index (MI) of inverter near unity to achieve the lowest total harmonic distortion (THD) of output voltage [9]. As can be seen from the experimental waveform, all the dc voltages are well controlled and maintained within $\pm 5\%$ of their nominal dc value.

Fig. 10 shows the experimental waveform of transformer-less UPFC operated at Case B: $\delta_s = 2^\circ$: (a) transmission line current I_{La} , sending-end current I_{Ca} and shunt current I_{pa} , and (b) V_{inv_ab} and I_{La} . In this case, since the power δ_s is reduced significantly, the resulted line current $I_L = 7\text{ A}$, active power $P = 0.14\text{ MW}$, and reactive power $Q = 0.07\text{ MVar}$. In addition, Fig. 11 shows averaged dc link voltage for both series and shunt CMI. Because much higher output voltage of series CMI is needed to compensate the phase angle difference, the dc voltage reference for series CMI changed from 450 V to 600 V, and the voltage reference for shunt CMI remains at 550 V.

Fig. 12 shows the transmitted P/Q between operating points A and B. The transformer-less UPFC can smoothly regulate the power through the transmission line from low (5%) to high (100%), or vice versa.

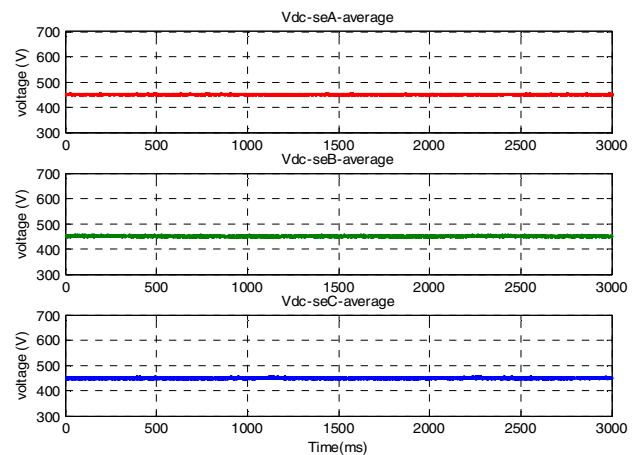


(a)

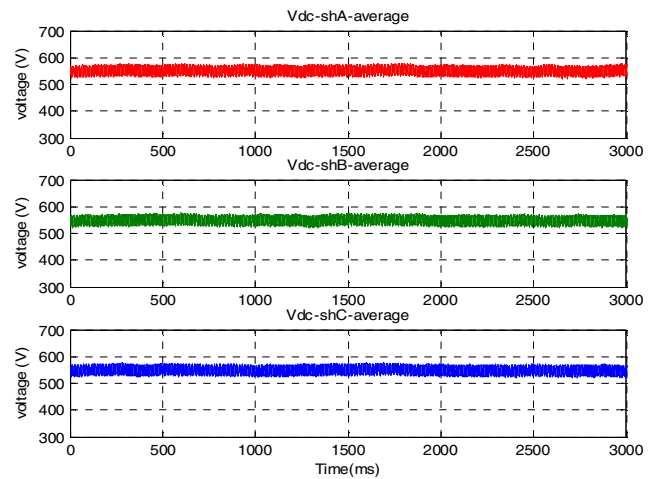


(b)

Fig. 8. Experimental waveform of UPFC operating at Case A: $\delta_s = 22^\circ$: (a) transmission line current I_{La} , sending-end current I_{Ca} and shunt current I_{pa} , and (b) V_{inv_ab} and I_{La} .

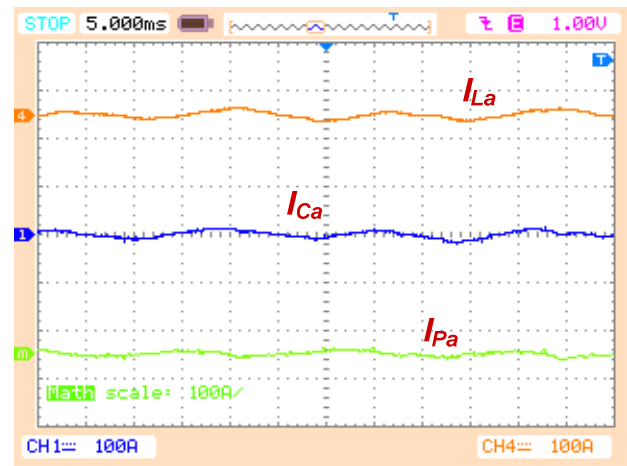


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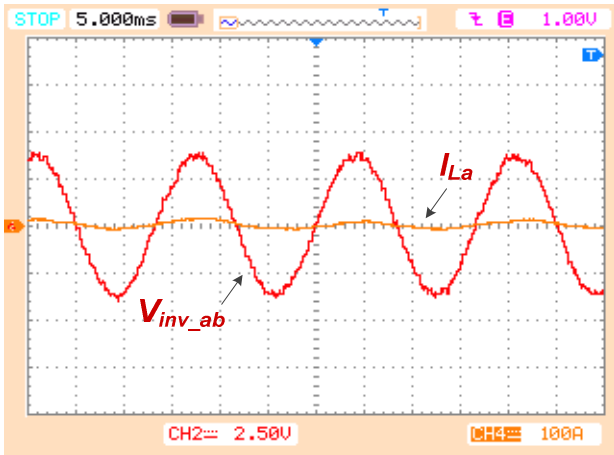


(b)

Fig. 9. Experimental results of average dc capacitor voltage of (a) series CMI and (b) shunt CMI, operating at Case A.

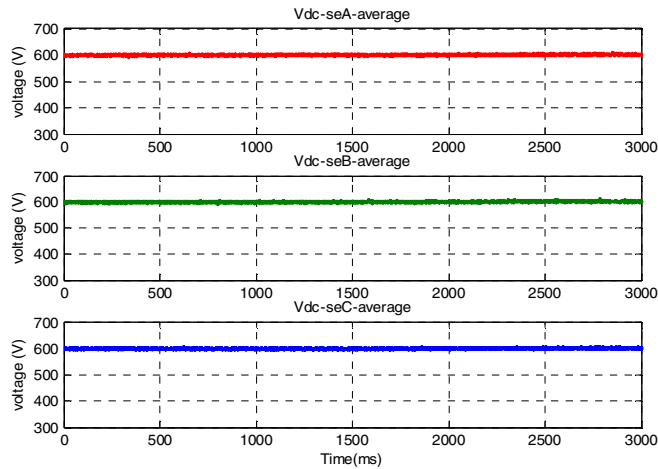


(a)

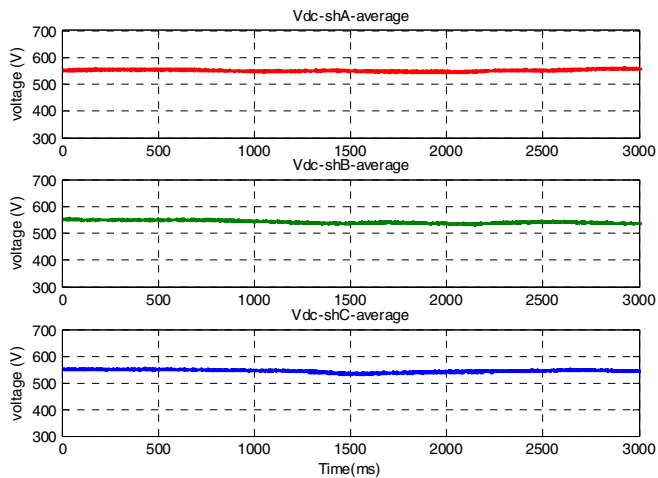


(b)

Fig. 10. Experimental waveform of UPFC operating at Case B: $\delta_s = 2^\circ$: (a) transmission line current I_{La} , sending-end current I_{Ca} and shunt current I_{pa} , and (b) V_{inv_ab} and I_{La} .



(a)



(b)

Fig. 11. Experimental results of average dc capacitor voltage of (a) series CMI and (b) shunt CMI, operating at Case B.

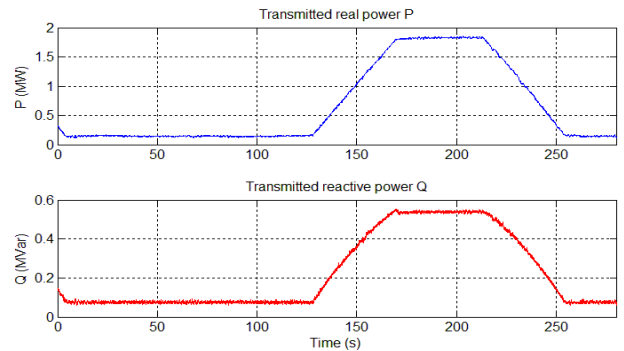


Fig. 12. Experimental results of P/Q between operating points A and B.

V. CONCLUSIONS

In this paper, the transformer-less UPFC is proposed for interconnection between two synchronous grids. The active power as well as the reactive power can be independently controlled by the new transformer-less UPFC. In addition, the system semiconductor device ratings (SSDPR) for different power flow control solutions have been investigated. It can be found that cascade multilevel inverter based transformer-less UPFC has much lower SDPR when compared to MMLC based back-to-back HVDC system. Compared to HVDC solution for interconnecting two synchronous grids, the transformer-less UPFC has much lower system rating, indicating significant cost saving. Experimental results based on 13.8 kV/ 2MVA transformers-less UPFC prototype are shown to validate the theoretical analysis.

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