A Single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit With Reduced Number of Power Switches

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***Abstract*—In this paper, a new single-phase cascaded multilevel inverter is proposed. This inverter is comprised of a series connection of the proposed basic unit and is able to only generate positive levels at the output. Therefore, an H-bridge is added to the proposed inverter. This inverter is called the developed cascaded multilevel inverter. In order to generate all voltage levels (even and odd) at the output, four different algorithms are proposed to determine the magnitude of dc voltage sources. Reduction in the number of power switches, driver circuits, and dc voltage sources is the advantage of the developed single-phase cascaded multilevel inverter. As a result, the installation space and cost of the inverter are reduced. These features are obtained by the comparison of the conventional cascaded multilevel inverters with the proposed cascaded topology. The ability of the proposed inverter to generate all voltage levels (even and odd) is reconfirmed by using the experimental results of a 15-level inverter.**

***Index Terms*—Basic unit, cascaded multilevel inverter, developed cascaded multilevel inverter, H-bridge.**

I. Introduction

THE demand for high-voltage high-power inverters is increasing, and it is impossible to connect a power semiconductor switch to a high-voltage network directly. Therefore, multilevel inverters had been introduced and are being developed now. With an increasing number of dc voltage sources in the input side, a sinusoidallike waveform can be generated at the output. As a result, the total harmonic distortion (THD) decreases, and the output waveform quality increases, which are the two main advantages of multilevel inverters. In addition, lower switching losses, lower voltage stress of dv/dt on switches, and better electromagnetic interference are the other most important advantages of multilevel inverters [1]–[5]. These kinds of inverters are generally divided into three main categories, i.e., neutral-point-clamped multilevel inverters, flying capacitor multilevel inverters, and cascaded multilevel inverters [6]–[9]. There is no diode clamped or flying capacitors in cascaded multilevel inverters. Moreover, these inverters consist of modularity, simplicity of control, and reliability, and they require the lowest number of power semiconductor devices to generate a particular level [1], [10], [11]. As a result, the losses and total cost of these inverters decrease, and the efficiency will increase [12]. These inverters are comprised of a series connection of basic units, which consist of different arrays of power switches and dc voltage sources. Generally, these inverters are divided into two main groups, i.e., symmetric cascaded multilevel inverters with the same amplitude of dc voltage sources and asymmetric cascaded multilevel inverters. The asymmetric cascaded multilevel inverters generate a higher number of output levels in comparison with the symmetric cascaded multilevel inverters with the same number of power electronic devices because of the different amplitude of its dc voltage sources. As a result, the installation space and total cost of an asymmetric cascaded multilevel inverter is lower than that of a symmetric cascaded multilevel inverter [11], [12].

Up to now, different basic units and, thus, different cascaded multilevel inverters have been presented in literature. In [13]–[18], different symmetric cascaded multilevel inverters have been presented. Another topology with two different algorithms as symmetric and asymmetric inverters have been also presented in [19]. The main disadvantages of the symmetric inverters are the high required numbers of power switches, insulated-gate bipolar transistors (IGBTs), power diodes, and

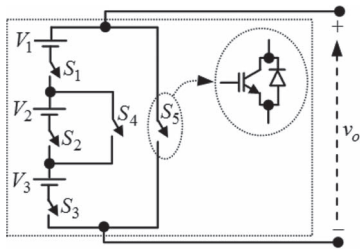

Fig. 1. Proposed basic unit.

TABLE I
PERMITTED TURN ON AND OFF STATES FOR SWITCHES IN THE PROPOSED BASIC UNIT

state	Switches state					v_o
	S_1	S_2	S_3	S_4	S_5	
1	off	off	off	off	on	0
2	on	off	on	on	off	V_1+V_3
3	on	on	on	off	off	$V_1+V_2+V_3$

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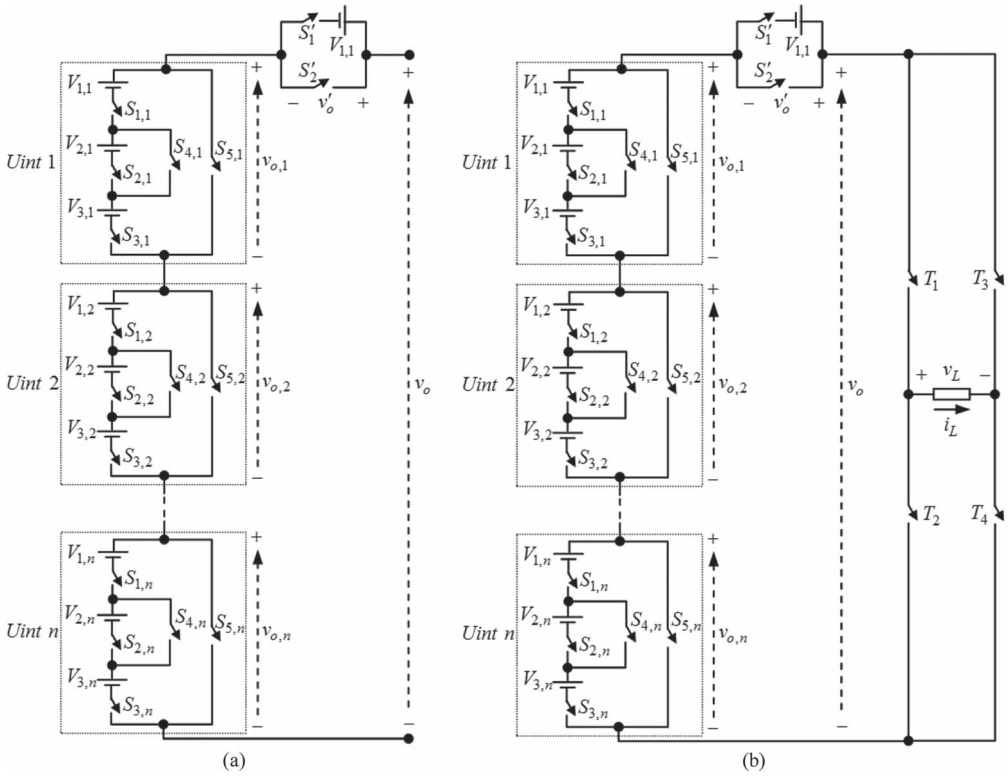

Fig. 2. Cascaded multilevel inverter. (a) Proposed topology. (b) Developed proposed topology.

driver circuits because of the same magnitude of dc voltage sources. These disadvantages will be higher in topologies where bidirectional power switches from the voltage point of view have been used, as presented in [15] and [19]. Each unidirectional switch requires an IGBT with an antiparallel diode and a driver circuit, whereas a bidirectional switch includes two IGBTs, two antiparallel diodes, and one driver circuit if a common emitter configuration is used. However, both unidirectional and bidirectional power switches conduct current in both directions. In order to increase the number of output levels, different asymmetric cascaded multilevel inverters have been presented in [12], [14], [19], and [20]. The main disadvantages of these inverters are the high magnitudes of dc voltage sources.

In order to increase the number of generated output levels by using a lower number of power electronic devices, a new basic unit is proposed in this paper. By a series connection of several proposed basic units, a new cascaded multilevel inverter is proposed. Then, to generate all positive and negative levels at the output, an H-bridge will be added to this inverter because the proposed inverter only generates positive levels. This inverter is called the developed proposed cascaded multilevel inverter. In order to generate all voltage levels at the output, four different algorithms are proposed. Several comparisons are also done between the developed cascaded multilevel inverter and its proposed algorithms with the conventional cascaded inverters. Based on these comparisons, the developed cascaded inverter requires the minimum number of power switches, IGBTs, power diodes, driver circuits, and dc voltage sources. Finally, in order to investigate the capability of the developed cascaded inverter to generate all voltage levels, the experimental results of a 15-level inverter are used.

II. Proposed Topology

Fig. 1 shows the proposed basic unit. As shown in Fig. 1, the proposed basic unit is comprised of three dc voltage sources and five unidirectional power switches. In the proposed structure, power switches (S_2, S_4), (S_1, S_3, S_4, S_5), and (S_1, S_2, S_3, S_5) should not be simultaneously turned on to prevent the short circuit of dc voltage sources. The turn on and off states of the power switches for the proposed basic unit are shown in Table I, where the proposed basic unit is able to generate three different levels of 0, $V_1 + V_3$, and $(V_1 + V_2 + V_3)$ at the output. It is important to note that the basic unit is only able to generate positive levels at the output.

It is possible to connect n number of basic units in series. As this inverter is able to generate all voltage levels except V_1, it is necessary to use an additional dc voltage source with the amplitude of V_1 and two unidirectional switches that are connected in series with the proposed units. The proposed cascaded inverter that is able to generate all levels is shown in Fig. 2(a). In this inverter, power switches S_1' and S_2' and dc voltage source V_1 have been used to produce the lowest output level. The amplitude of this dc voltage source is considered $V_1 = V_{\rm dc}$ (equal to the minimum output level). The output voltage level of each unit is indicated by $v_{o,1}$, $v_{o,2}, \ldots, v_{o,n}$, and v_o'. The output voltage level v_o of the proposed cascaded multilevel inverter is equal to

$$v_o(t) = v_{o,1}(t) + v_{o,2}(t) + \cdots + v_{o,n}(t) + v_o'(t). \quad (1)$$

The generated output voltage levels of the proposed inverter are shown in Table II. As aforementioned and according to Table II, the proposed inverter that is shown in Fig. 2(a) is only able to

TABLE II
GENERATED OUTPUT VOLTAGE LEVELS v_o BASED ON THE OFF AND ON STATES OF POWER SWITCHES

v_o	S'_1	S'_2	$S_{1,1}$	$S_{2,1}$	$S_{3,1}$	$S_{4,1}$	$S_{5,1}$	$S_{1,2}$	$S_{2,2}$	$S_{3,2}$	$S_{4,2}$	$S_{5,2}$	$\cdots$	$S_{1,n}$	$S_{2,n}$	$S_{3,n}$	$S_{4,n}$	$S_{5,n}$
0	off	on	off	off	off	off	on	off	off	off	off	on	$\cdots$	off	off	off	off	on
V_1	on	off	off	off	off	off	on	off	off	off	off	on	$\cdots$	off	off	off	off	on
$V_{1,1}+V_{3,1}$	off	on	on	off	on	on	off	off	off	off	off	on	$\cdots$	off	off	off	off	on
$V_{1,1}+V_{2,1}+V_{3,1}$	off	on	on	on	on	off	off	off	off	off	off	on	$\cdots$	off	off	off	off	on
$V_{1,2}+V_{3,2}$	off	on	off	off	off	off	on	on	off	on	on	off	$\cdots$	off	off	off	off	on
$V_{1,2}+V_{2,2}+V_{3,2}$	off	on	off	off	off	off	on	on	on	on	off	off	$\cdots$	off	off	off	off	on
$V_{1,1}+V_{1,2}+V_{1,3}+V_{2,1}+V_{2,3}$	off	on	on	on	on	off	off	on	off	on	on	off	$\cdots$	off	off	off	off	on
$V_{1,1}+V_{1,2}+V_{1,3}+V_{2,1}+V_{2,2}+V_{2,3}$	off	on	on	on	on	off	off	on	on	on	off	off	$\cdots$	off	off	off	off	on
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
$\sum_{j=1}^{n}(V_{1,j}+V_{2,j}+V_{3,j})$	off	on	on	on	on	off	off	on	on	on	off	off	$\cdots$	off	off	off	off	on
$V_{1,1}+\sum_{j=1}^{n}(V_{1,j}+V_{2,j}+V_{3,j})$	on	off	on	on	on	off	off	on	on	on	off	off	$\cdots$	off	off	off	off	on

TABLE III
PROPOSED ALGORITHMS AND THEIR RELATED PARAMETERS

Proposed algorithm	Magnitude of dc voltage sources	N_{level}	$V_{o,\max}$	V_{block}
First proposed algorithm (P_1)	$V_{1,j}=V_{2,j}=V_{3,j}=V_{dc}$ for $j=1, 2, \cdots, n$	$6n+3$	$(3n+1)V_{dc}$	$(21n+6)V_{dc}$
Second proposed algorithm (P_2)	$V_{1,1}=V_{2,1}=V_{3,1}=V_{dc}$, $V_{1,j}=V_{2,j}=V_{3,j}=2V_{dc}$ for $j=2, 3, \cdots, n$	$12n-3$	$6n-2$	$(40n-13)V_{dc}$
Third proposed algorithm (P_3)	$V_{1,1}=V_{2,1}=V_{3,1}=V_{dc}$, $V_{1,j}=\frac{1}{3}V_{2,j}=V_{3,j}=3^{j-2}V_{dc}$ for $j=2, 3, \cdots, n$	$5(3^{n-1})+4$	$\left[\frac{5(3^{n-1})+3}{2}\right]V_{dc}$	$[82(3^{n-1})-7]V_{dc}$
Fourth proposed algorithm (P_4)	$V_{1,j}=0.5V_{2,j}=V_{3,j}=2^{j-1}V_{dc}$ for $j=1, 2, \cdots, n$	$2^{n+3}-5$	$(2^{n+2}-3)V_{dc}$	$[7(2^{n+2})-22]V_{dc}$

generate positive levels at the output. Therefore, an H-bridge with four switches T_1–T_4 is added to the proposed topology. This inverter is called the developed cascaded multilevel inverter and is shown in Fig. 2(b). If switches T_1 and T_4 are turned on, load voltage v_L is equal to v_o, and if power switches T_2 and T_3 are turned on, the load voltage will be $-v_o$. For the proposed inverter, the number of switches N_{switch} and the number of dc voltage sources N_{source} are given by the following equations, respectively,

$$N_{\text{switch}} = 5n + 6 \tag{2}$$

$$N_{\text{source}} = 3n + 1 \tag{3}$$

where n is the number of series-connected basic units. As the unidirectional power switches are used in the proposed cascaded multilevel inverter, the number of power switches is equal to the numbers of IGBTs, power diodes, and driver circuits.

The other main parameter in calculating the total cost of the inverter is the maximum amount of blocked voltage by the switches. If the values of the blocked voltage by the switches are reduced, the total cost of the inverter decreases [12]. In addition, this value has the most important effect in selecting the semiconductor devices because this value determines the voltage rating of the required power devices. Therefore, in order to calculate this index, it is necessary to consider the amount of the blocked voltage by each of the switches. According to Fig. 2(b), the values of the blocked voltage by switches are equal to

$$V_{S'1} = V_{S'2} = V_{1,1} \tag{4}$$

$$V_{S1,j} = V_{S3,j} = \frac{V_{1,j} + V_{2,j} + V_{3,j}}{2} \tag{5}$$

$$V_{S4,j} = V_{S2,j} = V_{2,j} \tag{6}$$

$$V_{S5,j} = V_{1,j} + V_{2,j} + V_{3,j} \tag{7}$$

$$V_{T1} = V_{T2} = V_{T3} = V_{T4} = V_{o,\max} \tag{8}$$

where $V_{o,\max}$ is the maximum amplitude of the producible output voltage. Therefore, the maximum amount of the blocked voltage in the proposed inverter V_{block} is equal to

$$V_{\text{block}} = \sum_{j=1}^{n} V_{\text{block},j} + V'_{\text{block}} + V_{\text{block,H}}. \tag{9}$$

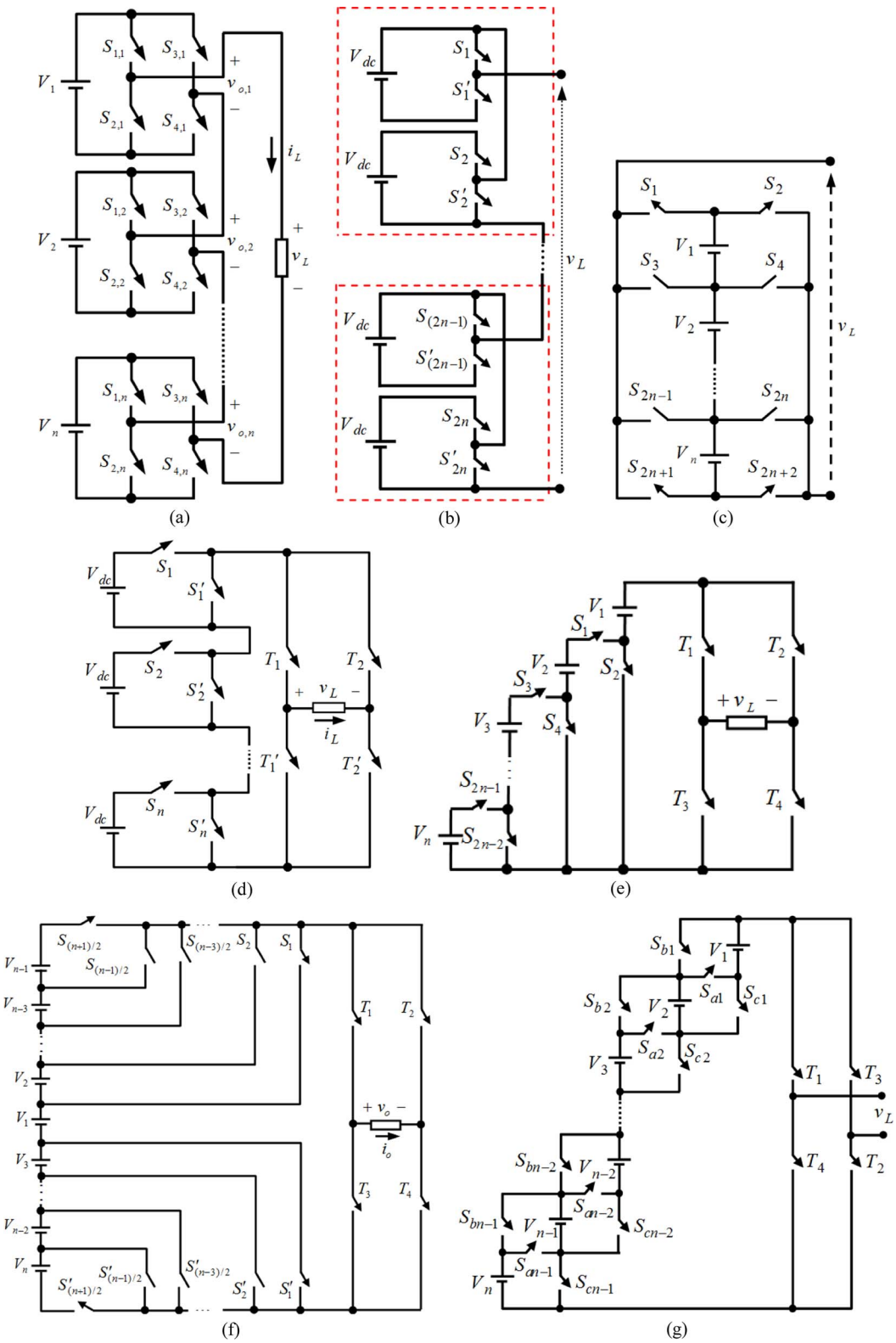

Fig. 3. Cascaded multilevel inverters. (a) Conventional cascaded multilevel inverter R_2 for $V_1 = V_2 = \cdots = V_n = V_{\rm dc}$ [14], R_3 for $V_1 = V_{\rm dc}$, $V_2 = \cdots = V_n = 2V_{\rm dc}$ [12], and R_4 for $V_1 = V_{\rm dc}$, $V_2 = \cdots = V_n = 3V_{\rm dc}$ [20]. (b) Presented topology in [17], with R_7 for $V_1 = V_2 = \cdots = V_n = V_{\rm dc}$. (c) Presented topology in [19], with R_8 for $V_1 = V_2 = \cdots = V_n = V_{\rm dc}$ and R_9 for $V_1 = V_{\rm dc}$, $V_2 = \cdots = V_n = 2V_{\rm dc}$. (d) Presented topology in [18] with R_{10}. (e) Presented topology in [16], with R_6 for $V_1 = V_2 = \cdots = V_n = V_{\rm dc}$. (f) Presented topology in [15], with R_5 for $V_1 = V_2 = \cdots = V_n = V_{\rm dc}$. (g) Presented topology in [13], with R_1 for $V_1 = V_2 = \cdots = V_n = V_{\rm dc}$.

In (9), $V_{{\rm block},j}$, $V'_{\rm block}$, and $V_{{\rm block,H}}$ indicate the blocked voltage by the jth basic unit, the additional dc voltage sources, and the used H-bridge, respectively.

In the developed inverter, the number and maximum amplitude of the generated output levels are based on the value of the used dc voltage sources. Therefore, four different algorithms

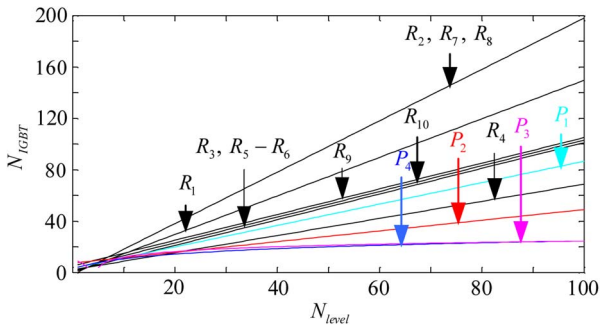

Fig. 4. Variation of N_{IGBT} versus N_{level}.

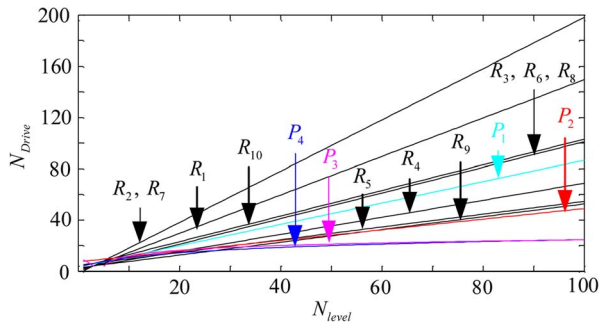

Fig. 5. Variation of N_{driver} versus N_{level}.

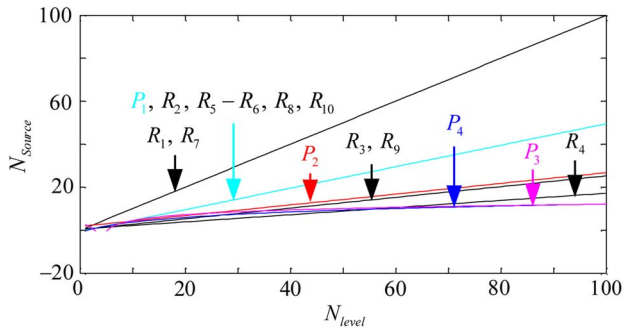

Fig. 6. Variation of N_{source} versus N_{level}.

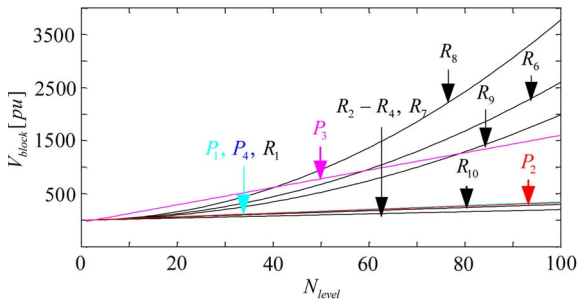

Fig. 7. Variation of V_{block} versus N_{level}.

are proposed to determine the magnitude of the dc voltage sources. These proposed algorithms and all their parameters are calculated and shown in Table III. According to the fact that the magnitudes of all proposed algorithms except the first algorithm are different, the proposed cascaded multilevel inverter based on these algorithms is considered an asymmetric cascaded multilevel inverter. In addition, based on the equations of the maximum output voltage levels and its maximum amplitude, it is clear that these values in the asymmetric cascaded multilevel inverter are more than those in the symmetric cascaded multilevel inverters with the same number of used dc voltage sources and power switches.

III. Comparing the Proposed Topology With the Conventional Topologies

The main aim of introducing the developed cascaded inverter is to increase the number of output voltage levels by using the minimum number of power electronic devices. Therefore, several comparisons are done between the developed proposed topology and the conventional cascaded inverters from the numbers of IGBTs, driver circuits, and dc voltage sources points of view. In addition, the maximum amount of the blocked voltage by the power switches is also compared between the proposed inverter and the other presented topologies. In this comparison, the proposed cascaded inverter that is shown in Fig. 2(b) with its proposed algorithms is represented by P_1 to P_4, respectively. In [13], a symmetric cascaded multilevel inverter has been presented that is shown by R_1 in this comparison. The H-bridge cascaded multilevel inverter has been presented in [14]. This inverter is represented by R_2. In addition, two other algorithms have been presented for the H-bridge cascaded inverter in [12] and [20] that are represented

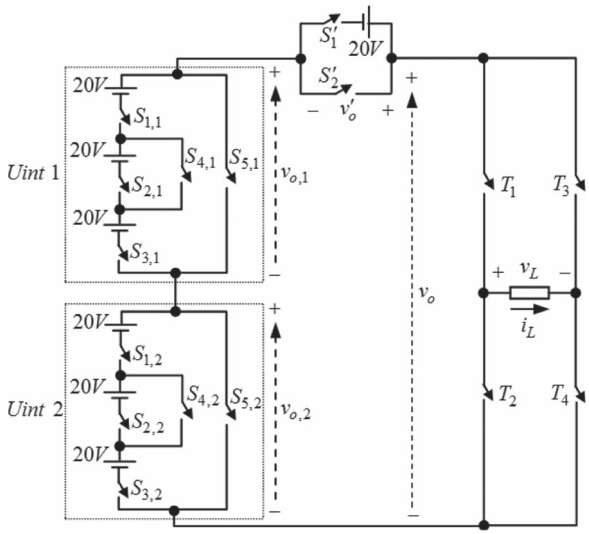

Fig. 8. Cascaded 15-level inverter based on the proposed basic unit.

by R_3 and R_4, respectively. In [15]–[17], three other symmetric cascaded multilevel inverters have been presented. These inverters are shown by R_5–R_7, respectively. The other cascaded multilevel inverter with two different algorithms has been presented in [19]. This inverter with its algorithms is represented by R_8 and R_9, respectively. Another symmetric cascaded multilevel inverter that has been presented in [18] is represented by R_{10} in this comparison. Fig. 3 indicates all of the aforementioned cascaded multilevel inverters.

Fig. 4 compares the number of IGBTs of the proposed topology with the other aforementioned cascaded multilevel inverters. As it is obvious, the proposed inverter needs a lower number of IGBTs to generate a specific level. In addition, the fourth proposed algorithm has the best performance among all

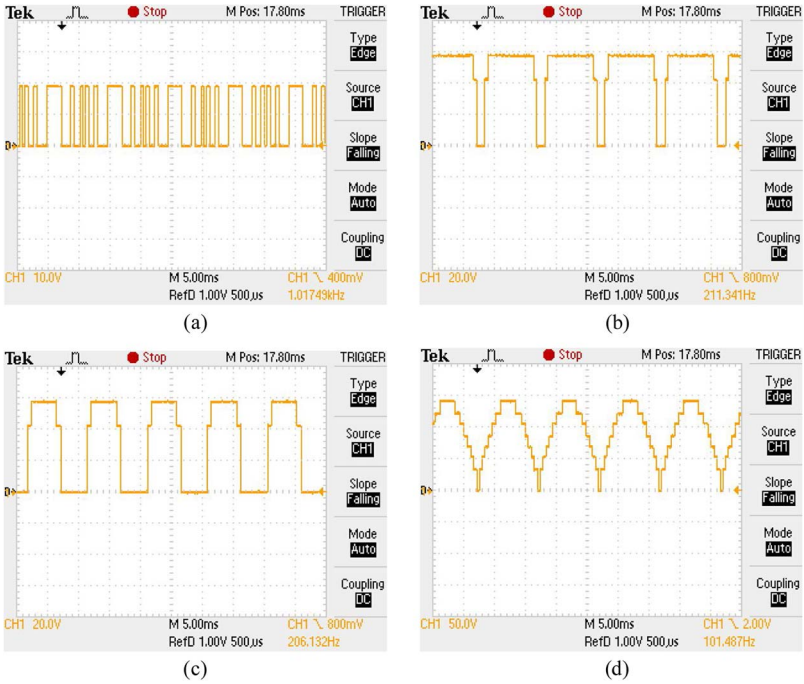

Fig. 9. Output voltage waveforms of each unit. (a) v_o'. (b) $v_{o,1}$. (c) $v_{o,2}$. (d) v_o.

of the proposed algorithms for the developed cascaded inverter. However, in this comparison, the unidirectional power switches have been used in many of the considered cascaded inverters. As aforementioned, the number of used IGBTs is equal to the number of power diodes. As a result, the number of required power diodes in the fourth proposed algorithm of the developed topology is lower than that of the other aforementioned inverters and their proposed algorithms.

Fig. 5 indicates the comparison of the proposed cascaded inverter with other aforementioned topologies from the point of view of the number of driver circuits. As each switch requires a separate driver circuit, the number of driver circuits is equal to the number of power switches. Therefore, this comparison also indicates the number of required power switches in the cascaded multilevel inverters. As shown in Fig. 5, the number of driver circuits based on the fourth proposed algorithm of the developed cascaded inverter is lower than that of the other proposed algorithms for this inverter and other aforementioned cascaded inverters.

Fig. 6 compares the number of dc voltage sources of the proposed topology with the other aforementioned cascaded inverters. As it is obvious, the number of required dc voltage sources in the developed inverter is less than that in the other presented inverters in literature. This difference will be higher while the fourth proposed algorithm is considered.

Fig. 7 compares the maximum amount of the blocked voltage by the power switches in the proposed topology with the other aforementioned inverters. As it is obvious, this value in the proposed inverter is less than that in the other presented inverters except the H-bridge inverter and presented topologies by R_7 and R_{10}. However, this is the main disadvantage of the proposed cascaded inverter, but this inverter has different advantages in comparison to the H-bridge cascaded inverter and the presented topologies by R_7 and R_{10}, such as its required lower

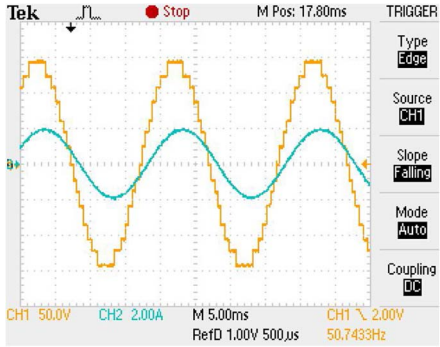

Fig. 10. Waveforms of the load voltage and current.

numbers of IGBTs, driver circuits, and dc voltage sources. It is pointed out that all values are considered in per unit (p.u.), and $V_{\rm dc}$ is used as the base value in the per-unit system.

As it is obvious from the aforementioned comparisons, the developed proposed inverter has the best performance among all of the aforementioned multilevel topologies. Reduction in the numbers of required IGBTs, power diodes, driver circuits, and dc voltage sources, and the amount of the blocked voltage by the power switches are remarkable advantages of the proposed inverter that were obtained from comparisons. These advantages lead to reduction in the installation space and total cost of the inverter. These features will have the most influence when the fourth proposed algorithm is used.

IV. Experimental Results

In order to clarify the correct performance of the developed proposed inverter in generating the desired output voltage levels, the experimental results have been used. The number of required power electronic devices in the proposed inverter

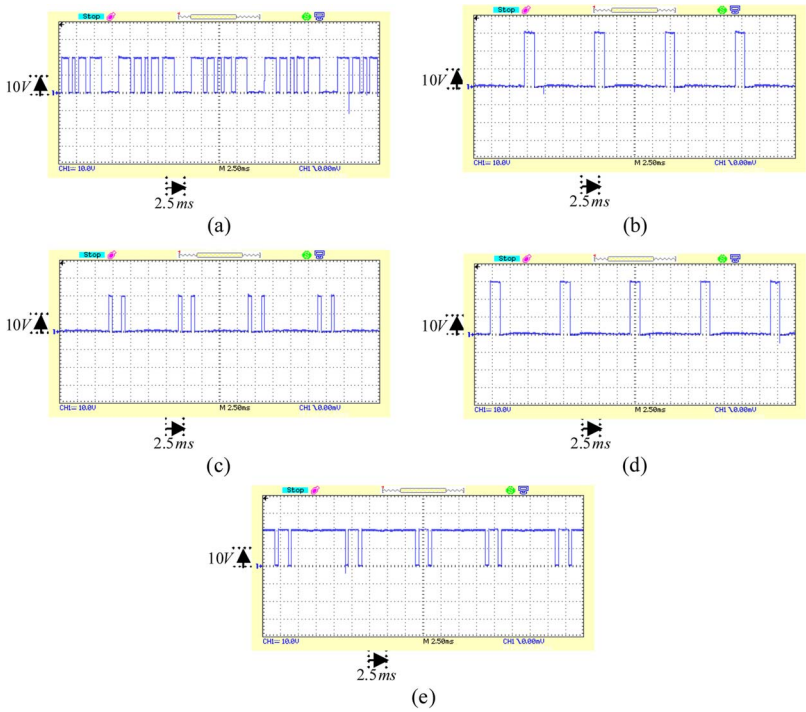

Fig. 11. Voltage on switches. (a) S'_1. (b) $S_{1,1}$. (c) $S_{2,1}$. (d) $S_{3,1}$. (e) $S_{4,1}$.

is completely based on the selected algorithm to determine the magnitude of the dc voltage sources. In this section, the investigations are done on a cascaded multilevel inverter that is shown in Fig. 8. This inverter consists of two proposed basic units and one additional series-connected dc voltage source that lead to the use of 7 dc voltage sources and 12 unidirectional power switches. The first proposed algorithm is considered to determine the magnitude of the dc voltage sources with $V_{\rm dc}=20$ V. According to (5), this inverter is able to generate 15 levels (seven positive levels, seven negative levels, and one zero level) with the maximum amplitude of 140 V at the output. It is important to note that the used IGBTs on the prototype are BUP306D (with an internal antiparallel diode). The 89C52 microcontroller by ATMEL Company has been used to generate all switching patterns. In all processes of the experimental performance, the load is assumed as a resistive–inductive $(R-L)$ load, with $R=70\ \Omega$, and $L=55$ mH. It is important to point out that the used control method in this inverter is the fundamental control method. The main reason to select this control method is its low switching frequency compared with other control methods that leads to reduction in switching losses.

Fig. 9 shows the experimental results. As it is obvious in this figure, this inverter is only able to generate positive levels at the output. Fig. 9(a) shows that the added dc voltage source generates the minimum magnitude of the output levels that is equal to the lower value of the used dc voltage sources. Fig. 9(b) and (c) indicates that each unit generates the output voltage levels of 0, 40, and 60 V. By adding an H-bridge, this inverter is able to generate all positive and negative levels at the output. Fig. 10 shows the waveforms of the load voltage and current. As shown in Fig. 10, this inverter generates a step waveform with 15 levels and a maximum amplitude of 140 V. By comparing the current and voltage waveforms, it is clear that the current waveform is near the ideal sinusoidal waveform and consists of a phase shift in comparison with the load voltage. These differences are due to the resistive–inductive load feature that acts as a low-pass filter.

As aforementioned, the used power switches on the developed inverter are unidirectional switches; therefore, in order to verify this fact, the voltages on the switches S'_1, $S_{1,1}$, $S_{2,1}$, $S_{3,1}$, and $S_{4,1}$ of the first proposed unit are indicated in Fig. 11. It is noticeable that the waveforms of the voltage across S'_2 and $S_{5,1}$ are the same as those across v'_o and $v_{o,1}$, respectively. As shown in this figure, the magnitude of the blocked voltages on the switches are either positive or zero, and there is no negative amount on them. This fact reconfirms the existence of unidirectional power switches in this topology.

V. Conclusion

In this paper, a new basic unit for a cascaded multilevel inverter is proposed. By the series connection of several basic units, a cascaded multilevel inverter that only generates positive levels at the output is proposed. Therefore, an H-bridge is added to the proposed inverter to generate all voltage levels. This inverter is called the developed cascaded multilevel inverter. In order to generate even and odd voltage levels at the output, four different algorithms are proposed to determine the magnitude of the dc voltage sources. Then, several comparisons are done between the developed proposed single-phase cascaded inverter and its proposed algorithms with cascaded multilevel inverters that have been proposed in literature. According to these comparisons, the developed proposed cascaded topology requires less numbers of IGBTs, power diodes, driver circuits, and dc voltage sources than other presented cascaded topologies in literature. These features will

be remarkable while the fourth proposed algorithm is used for the developed cascaded inverter. For instance, in order to generate a minimum of 63 levels at the output, the developed cascaded topology based on the fourth proposed algorithm needs 19 power diodes, IGBTs, and driver circuits, and 10 dc voltage sources. However, the cascaded multilevel inverter that was presented in [20] requires 44 power diodes, IGBTs, and driver circuits, and 11 dc voltage sources. Therefore, the developed proposed inverter has better performance and needs minimum number of power electronic devices that lead to reduction in the installation space and total cost of the inverter. Finally, the accuracy performance of the developed proposed single-phase cascaded multilevel inverter in generating all voltage levels is verified by using the experimental results on a 15-level inverter.

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