# A New Hybrid Active Neutral Point Clamped Flying Capacitor Multilevel Inverter

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***Abstract*—This paper proposes a new five-level hybrid topology combining features of neutral point clamped and flying capacitor inverters. The proposed topology provides a tradeoff between different component counts to achieve a good loss distribution, avoid direct series connection of semiconductor devices, keep the balanced operation of dc-link capacitors while keeping the number of costly components such as capacitors and switches low. The required modulation strategy is developed and the operation of the proposed topology is studied. The features of the proposed topology are investigated and compared to other available topologies. Simulation results are provided to verify the performance of the converter for medium voltage applications.**

***Keywords—Multilevel Inverter, Flying Capacitor, Active Neutral Point Clamped, Diode Clamped.***

## I. INTRODUCTION

Multilevel inverters have gained interest during the last three decades due to the increasing demand for medium to high voltage converters for a variety of high power applications. Different topologies have been proposed to fit the requirements of different applications. For medium voltage inverters, cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitor (FC) are the primary topologies. Among them, NPC and FC provide a common dc-link which is a strict requirement for many applications [1]–[6].

FC inverter uses capacitors to generate output voltage levels. The availability of intra-phasal redundant states in this topology can provide both capacitor voltage balancing and power loss distribution among switches [7]. However, increased number of flying capacitors at higher levels that increases the initial cost and maintenance surcharges and decreases the reliability of the inverter along with the capacitor precharge in some applications are the main drawbacks of this topology [8].

NPC inverter uses diodes to clamp the voltage levels generated at the dc-link capacitors to the output. Excessive number of diodes, unbalanced operation of dc-link's voltage divider capacitors, and uneven distribution of loss among switches are major problems of this topology. Space vector algorithms are available to alleviate the unbalanced loss and capacitor voltage problems based on the inverter's operating condition [5]. Active NPC (ANPC) improves the loss distribution of NPC by replacing diodes with active switches providing alternative neutral point path [9].

Hybrid topologies are viable solutions where higher number of levels is required. Combining the advantages of CHB, FC, and NPC, hybrid inverters can provide loss and voltage balancing while keeping the number of components low. Examples of hybrid topologies combining FC and NPC can be found in [10]–[12], some of which has already found industrial applications. The 5-level FC-ANPC is an example of hybrid topologies that made its way to the industry. The ACS2000 family of medium voltage drives, commercialized by ABB, uses this topology with both active and passive front end configurations. The main advantage of this topology is the use of a single flying capacitor to generate the output five levels. Compared to other topologies that provide a common dc-link, FC-ANPC has provided an acceptable tradeoff between the cost, performance, and reliability for 5-level applications. The disadvantages of FC-ANPC are high number of switches, series connection of high voltage switches, and poor loss distribution [13].

This paper proposes a new 5-level hybrid topology based on FC and NPC inverters. The goal of the proposed topology is to overcome the shortcomings of the traditional FC-ANPC. Thus, comparatively, the proposed topology provides better loss distribution, avoids direct series connection of high voltage switches, and eliminates 2 switches per phase leg. These advantages come at the cost of an additional capacitor and 6 diodes. Nevertheless, the lifetime of each capacitor is expected to prolong due to the half cycle operation and lower rms current.

In this paper, the configuration and operation of the proposed topology is described in section II. In section III, associated carrier-based and non-carrier-based modulation techniques are presented and modified to suit the proposed topology. Section IV provides a comparison between the proposed topology and other topologies that are available for 5-level configuration. In section V, the simulation result of a case study is presented to verify the operation of the proposed topology for medium voltage applications.

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## II. The Proposed Topology and Operation

The proposed topology includes a dc-link that is common among the three phases. The dc-link provides three voltage levels +2E, 0, and -2E for the phase legs. Since all the phases have similar configuration, only one phase leg of the proposed topology has been shown in Fig. 1. All the components shown in the figure have equal operating voltage E i.e. one fourth of the dc-link voltage $V_{dc}$. The flying capacitors $C_{A1}$ and $C_{A2}$ are controlled to stay charged at the target voltage E.

The available states of one phase leg are shown in table I. To generate level 2E, all the top arm switches $S_{A1}$, $S_{A2}$, $S_{A3}$, $S_{A4}$ should turn on. For level E, two choices are available i.e. either through dc-link's positive point (EP) or through dc-link's neutral point (E0). This redundancy can be used to balance the voltage of $C_{A1}$. Level 0 is generated through clamping the dc-link's neutral point to the output (00). Negative states can be generated similarly due to the symmetry of the topology.

The operation of this topology is in essence similar to topologies such as stacked multicell (SMC) converter [14], [15], [7], where the positive and negative stacks operate independently. Hence, the positive stack capacitor $C_{A1}$ is used and balanced during the positive cycle and rest during the negative cycle, whereas the negative stack capacitor $C_{A2}$ is used and balanced during the negative cycle and rest during the positive cycle. So, the flying capacitors will see the switching frequency rather than line frequency and therefore the capacitor size is not too large.

Similar to the three-level NPC inverter, if the three phases of the load are balanced, the neutral point voltage will be constant in theory. However, the voltage might slightly drift away due to the imbalance in the elements' leakage current. In addition, although small, there is always some imbalance among the phases. A constant voltage drift, even though small, can cause higher voltage across part of the devices which can be lethal. Nevertheless, this drift can be compensated by injecting a small common mode to the three phases.

An important feature of the proposed topology is the even distribution of transitions among switching devices. Therefore, switching loss which is the major limiting factor of inverter's thermal performance is distributed among the switches. As the main result, the tradeoff between switching frequency and current derating is improved. This provides the opportunity to either increase the rated current and power of the inverter or increase the switching frequency resulting in lower capacitor size and improved voltage waveform quality.

## III. Modulation Techniques

Various modulation techniques may be adapted for the proposed topology. Carrier-based modulation with sinusoidal or modified reference as well as non-carrier-based techniques such as space vector modulation and selective harmonic elimination may be used to generate the gate signals. The choice of a modulation technique is mostly a tradeoff among the requirements of the application, complexity of the software, and cost of the control hardware.

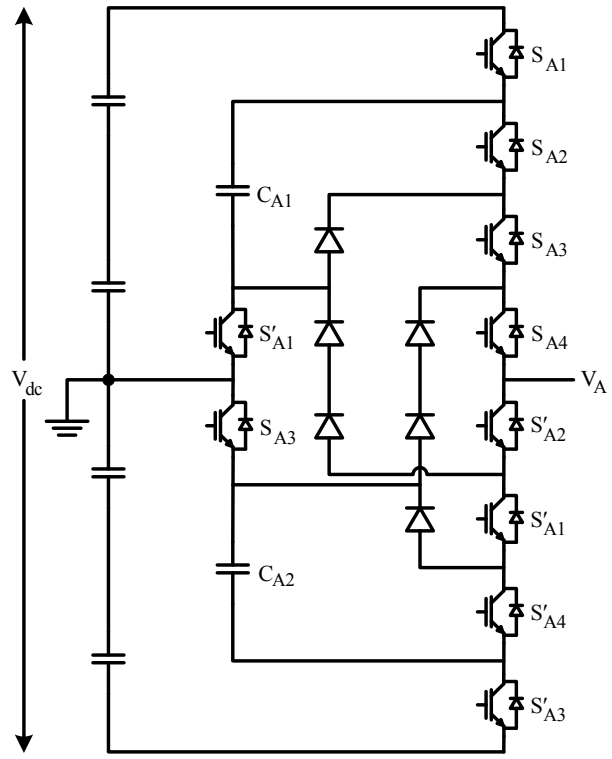


Fig. 1. A phase leg of the proposed 5-level hybrid topology.

TABLE I. Switching States of the Proposed Inverter

| Level | State | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $C_1$ | $C_2$ |
|---|---|---|---|---|---|---|---|
| +2E | +2E | 1 | 1 | 1 | 1 | N.A. | N.A. |
| +E | +EP | 1 | 0 | 1 | 1 | i>0 Charge<br>i<0 Discharge | N.A. |
| | +E0 | 0 | 1 | 1 | 1 | i>0 Discharge<br>i<0 Charge | N.A. |
| 0 | 0 | 0 | 0 | 1 | 1 | N.A. | N.A. |
| -E | -E0 | 0 | 0 | 1 | 0 | N.A. | i>0 Charge<br>i<0 Discharge |
| | -EN | 0 | 0 | 0 | 1 | N.A. | i>0 Discharge<br>i<0 Charge |
| -2E | -2E | 0 | 0 | 0 | 0 | N.A. | N.A. |

$S'_1$, $S'_2$, $S'_3$, $S'_4$ are switched complementary to $S_1$, $S_2$, $S_3$, $S_4$ respectively.
i>0 represents outbound current and i<0 represents inbound current.
N.A. stands for Not Affected

### *A. Carrier-Based Modulation*

Carrier set's arrangement and reference waveform's shape are the main sources of varieties in carrier-based modulation techniques for multilevel inverters.

As for carrier set's arrangement, level shifted carriers LSC and phase shifted carriers PSC are the two main categories that are respectively suitable for diode-clamped and multi-cell structures. Two members in the LSC family, alternative phase opposition disposition APOD and phase disposition PD are

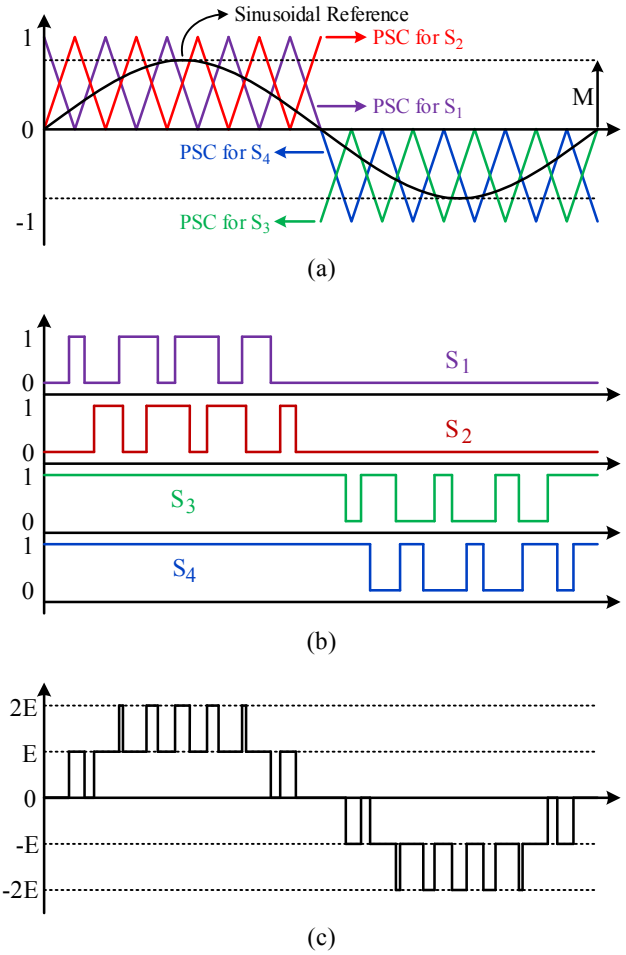


Fig. 2. Carrier-based modulation using PSC with sinusoidal reference for single phase application. (a) Reference and carriers arrangement. (b) Gate signals. (c) Output waveform.

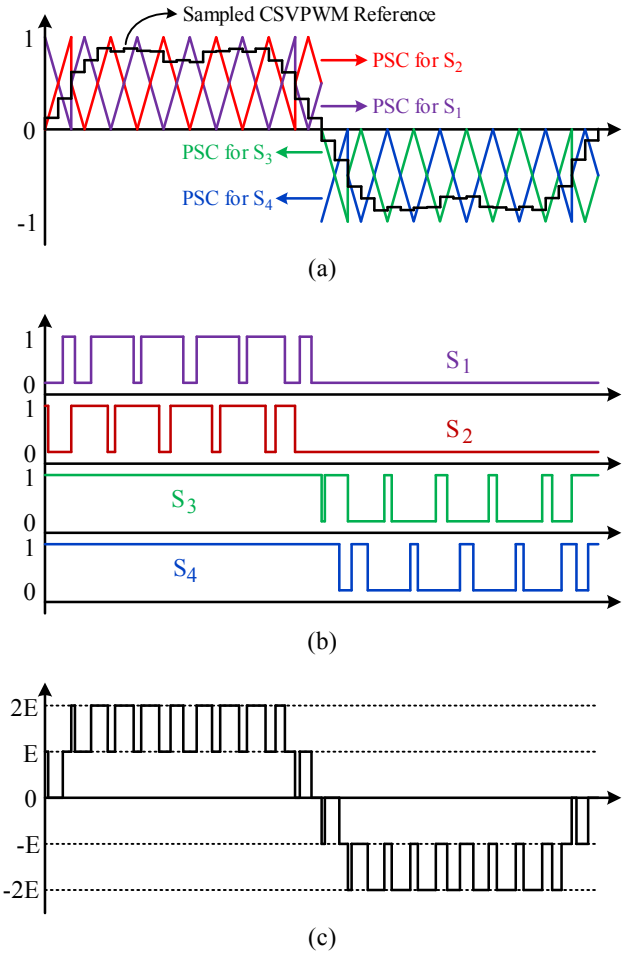


Fig. 3. Carrier-based modulation using modified PSC with sampled CSVPWM reference for three phase application. (a) Reference and carriers arrangement. (b) Gate signals. (c) Output waveform.

known to generate the best results for singe-phase and three-phase applications, respectively. PSC in its original form has been shown to generate a PWM waveform that matches with APOD. Also a modified version of PSC with dynamic phase shift has been shown to match with PD [16].

The reference for single-phase applications is usually a simple sinusoidal waveform. For three-phase applications, a variety of reference waveforms are available due to the possibility of common mode injection in three-phase structure. This flexibility has been used to serve different purposes such as increased dc link utilization, lower THD, lower Loss, and neutral point voltage control.

For the proposed inverter, a hybrid modulation technique is required due to the hybrid structure of the topology. Figure 3 illustrates the modulation technique for single-phase case. It is intuitive to separate the operation to positive and negative cycles, since each cycle is generated with a 3-level FC stack. The gate signals for each FC is then generated using PSC to provide natural voltage balancing for the flying capacitors. The generated output PWM waveform matches the APOD scheme.

For three-phase case, similar approach may be adopted except that, to generate a PD scheme equivalent, the positive cycle carriers should have $\pi/2$ phase shift compared to the negative cycle carriers. Also, the carriers incorporate a dynamic phase shift which for sampled reference waveforms always adds up by $\pi/2$ at the carrier band transitions. For the reference waveform, centered space vector PWM (CSVPWM) sampled at half PD carrier period can provide similar output performance as SVM. Figure 4 illustrates the modulation technique using sampled CSVPWM along with modified PSC for the proposed inverter.

### *B. Non-Carrier-Based Modulation*

For non-carrier-based modulation techniques such as SVM and SHE, the output PWM waveform may be generated first and then decomposed to the required switching signals. Figure 4 illustrates the required procedure to generate the gate signals for each phase leg. The 5-level PWM waveform is first separated to positive and negative cycle 3-level PWMs. Using state machine decoder, each cycle is then decomposed to two 2-level PWMs i.e. the required gate signals for each FC cell.

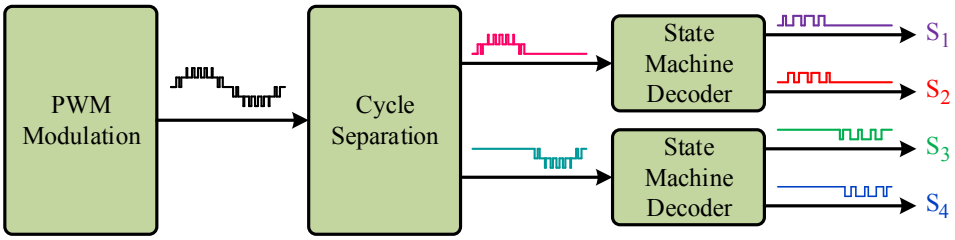


Fig. 4. Non-carrier-based modulation for a phase leg of the proposed inverter.

It is important to note that this procedure is independent of the adopted modulation technique. Therefore, it can be used with carrier-based modulation techniques as well as non-carrier-based. This might be a good alternative when the complexity of the carrier-based technique is relatively high e.g. for PD scheme.

## IV. Comparison with Other Topologies

A Comparison between the proposed topology and different 5-level topologies in terms of component count and loss distribution is listed in table II. The 5-level NPC has low switch count but the major problems are unbalanced operation of dc-link capacitors, poor loss distribution among switches, and excessive number of diodes. 5-Level FC provides low switch count and excellent loss distribution but requires high number of flying capacitors that can adversely affect the initial cost, maintenance and replacement surcharges, and reliability of the inverter. Capacitors' precharge requirement in some applications is also a drawback of this topology. The 5-level SMC topology provides lower capacitor count compared to FC and good loss distribution. However, high switch count and high frequency switches in series are the main issues of this topology. The 5-Level FC ANPC provides a good balance between the number of semiconductors and capacitors. The major issue with this topology is the poor loss distribution among the switches. The topology proposed in this paper, provides a tradeoff between different component counts to achieve a good loss distribution, avoid direct series connection of semiconductor devices, keep the balanced operation of dc-link capacitors while keeping the number of costly components such as capacitors and switches as small as possible.

TABLE II. Comparison of Different Topologies

| Topology | Flying Capacitors | Switches | Diodes | Loss Distribution |
|---|---|---|---|---|
| 5L-NPC | 0 | 8 | 12 | Poor |
| 5L-FC | 6 | 8 | 0 | Excellent |
| 5L-SMC | 2 | 12 | 0 | Good |
| 5L-FC-ANPC | 1 | 12 | 0 | Fair |
| Proposed Topology | 2 | 10 | 6 | Good |

The component counts in this table are per phase leg.

## V. Simulation Results

To verify the operation of the proposed topology and the performance of the modulation techniques provided in section III, a model is developed and simulated with PSIM software. The performance of the natural balancing technique for a three-phase 12kV inverter supplying a 5MVA load at power factor of 0.7 is shown in Fig. 5. Centered space vector modulation (CSVPWM) is used at modulation index of 1.09 and carrier

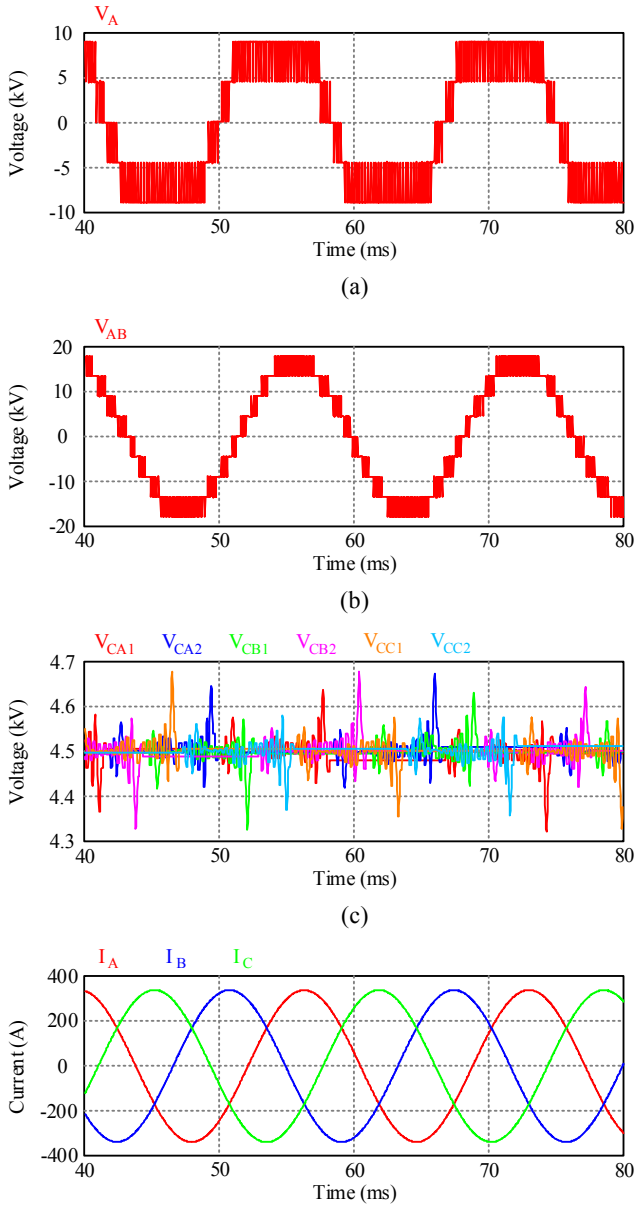


Fig. 5. Simulation results. (a) Phase voltage (b) Line voltage (c) Flying capacitor voltages (d) Load current

frequency 5kHz. The dc-link voltage is set at 18kV and flying capacitors are 330μF. It can be seen that even without an RLC balance booster, the capacitor voltage errors are limited to less than 4%.

## VI. Conclusion

A new hybrid 5-level inverter topology and modulation technique is proposed. Compared to 5-level ANPC as the most similar topology, this new topology requires two less switches at the cost of an additional capacitor and six diodes. However, since the capacitors still see the switching frequency and their size remain the same, it is expected to reduce the inverter's total cost. Also, unlike 5-level ANPC, all switches must withstand the same voltage which eliminates the need for series connection of switches and associated simultaneous turn on and off problem. Good loss distribution among switches can increase the inverters rated power or provide higher switching frequency and smaller capacitor size.

## References


[1] H. Abu-Rub, J. Holtz, and J. Rodriguez, "Medium-Voltage Multilevel Converters—State of the Art, Challenges, and Requirements in Industrial Applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2581–2596, Aug. 2010.

[2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, J. Rodriguez, M. A. Pérez, and J. I. Leon, "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[3] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A Survey on Cascaded Multilevel Inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[4] J. Rodriguez, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[5] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[6] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[7] B. P. McGrath, T. Meynard, G. Gateau, and D. G. Holmes, "Optimal Modulation of Flying Capacitor and Stacked Multicell Converters Using a State Machine Decoder," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 508–516, Mar. 2007.

[8] H. Sepahvand, M. Khazraei, K. Corzine, and M. Ferdowsi, "Start-up Procedure and Switching Loss Reduction for a Single-Phase Flying Capacitor Active Rectifier," *Ind. Electron. IEEE Trans.*, vol. 60, no. 9, pp. 3699–3710, May 2013.

[9] T. Bruckner, S. Bernet, and H. Guldner, "The Active NPC Converter and Its Loss-Balancing Control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 855–868, Jun. 2005.

[10] M. Narimani, B. Wu, Z. Cheng, and N. Zargari, "A New Nested Neutral Point Clamped (NNPC) Converter for Medium-Voltage (MV) Power Conversion," *IEEE Trans. Power Electron.*, vol. 8993, no. MV, pp. 1–1, 2014.

[11] S. R. Pulikanti and V. G. Agelidis, "Hybrid Flying-Capacitor-Based Active-Neutral-Point-Clamped Five-Level Converter Operated With SHE-PWM," *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4643–4653, Oct. 2011.

[12] T. B. Soeiro and J. W. Kolar, "The New High-Efficiency Hybrid Neutral-Point-Clamped Converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1919–1935, May 2013.

[13] F. Kieferndorf, M. Basler, L. a. Serpa, J.-H. Fabian, a. Coccia, and G. a. Scheuer, "A new medium voltage drive system based on ANPC-5L technology," *2010 IEEE Int. Conf. Ind. Technol.*, pp. 643–649, 2010.

[14] G. Gateau, T. A. Meynard, and H. Foch, "Stacked multicell converter (SMC): properties and design," in *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)*, 2001, vol. 3, pp. 1583–1588.

[15] T. A. Meynard, H. Foch, F. Forest, C. Turpin, F. Richardeau, L. Delmas, G. Gateau, and E. Lefeuvre, "Multicell converters: derived topologies," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 978–987, Oct. 2002.

[16] R. Naderi and A. Rahmati, "Phase-Shifted Carrier PWM Technique for General Cascaded Inverters," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1257–1269, May 2008.