A Three-Level *LC*-Switching-Based Voltage Boost NPC Inverter

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***Abstract*—A single-stage high-voltage gain boost inverter is getting popularity in applications like solar photovoltaic, fuel cell, uninterruptible power system (UPS) systems, etc. Recently, single-stage voltage boost multilevel Z-source inverter (ZSI) and quasi-Z-source inverter (QZSI) have been proposed for dc–ac power conversion with improved power quality. Multilevel ZSI uses more number of high-power passive components in the intermediate network, which increase the system size and weight. Also, its input current is discontinuous in nature which is not desirable in some of the applications like fuel cell, UPS systems, hybrid electric vehicle, etc. In this paper, a continuous current input three-level *LC*-switching-based voltage boost neutral-point-clamped inverter is proposed, which uses comparatively less number of high-power passive components at the same time retains all the advantages of multilevel QZSI/ZSI. It is able to boost the input dc voltage and give required three-level ac output voltage in a single stage. Steady-state analysis of the proposed inverter is discussed to formulate the relationship between the input dc voltage and three-level ac output voltage. A unipolar pulse width modulation technique devised for the proposed inverter to eliminate first center band harmonics is also presented. The proposed converter has been verified by simulation in MATLAB Simulink as well as performing experiment with the help of a laboratory prototype.**

***Index Terms*—Boost inverter, pulse width modulation (PWM), shoot through, three-level inverter, Z-source inverter (ZSI).**

NOMENCLATURE

$T_{\rm on}$	Shoot-through period.
T_s	Switching time period.
D	Shoot-through duty ratio (ratio of $T_{\rm on}$ to $T_{\rm s}$).
$V_{\rm dc}$	DC voltage fed before the inverter leg from dc side.
I_i	Average dc input current.
V_g	Input dc voltage.
V_m	Peak ac phase voltage at output.
M	Modulation index.
V_{C1}, V_{C2}	Voltages across the capacitors C_1, C_2, respectively.
I_{C1}, I_{C2}	Currents through the capacitors C_1, C_2, respectively.
V_{L1}, V_{L2}	Voltages across the inductors L_1, L_2, respectively.
I_{L1}, I_{L2}	Currents through the inductors L_1, L_2, respectively.

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I. INTRODUCTION

CURRENTLY, the multilevel voltage-source inverter (VSI) is used in a wide range of applications like photovoltaic (PV) system, uninterruptible power supply (UPS), fuel cell, wind power, hybrid electric vehicle (HEV), etc., [1]–[4]. The multilevel VSI provides advantages like better power quality, smaller output ac filter requirements, lower voltage stress across the inverter switches, etc. However, the conventional multilevel VSI behaves like buck converter [5], i.e., peak ac output voltage is less than the input dc-link voltage. In applications like PV system, fuel cell, UPS, etc., the required ac output voltage level is achieved by using either a dc–dc converter before the VSI or a transformer after the VSI [6], [7], but more number of power converter stages increases system control complexity and decreases the system efficiency [8]. Similarly, an inclusion of line frequency transformer increases the system size and weight [9]. In multilevel VSI, shoot-through (i.e., switching all the switches in the inverter leg) results dead short circuit of the source. Shoot through is avoided by providing dead band between switching control signal fed to the complementary switches of inverter leg, which introduces distortion in the output ac voltage.

The Z-source inverter (ZSI) addresses the above issues and is able to boost the input dc voltage to achieve the required ac voltage in a single stage [10]–[13]. Conventional three-level Z-source neutral-point-clamped (NPC) inverters are explored for medium-power and low-power applications [14], [15]. It provides better power quality at the same time voltage stress across switches and output filter requirements are less. This uses two isolated dc sources which may require isolation transformer and additional rectifier circuits (in case isolated dc sources are not readily available). It is primarily operated in three states, i.e., nonshoot-through state, zero state, and shoot-through state. In multilevel ZSI, shoot-through state is utilized along with passive reactive element to boost the input dc voltage. It is similar to the zero state of multilevel VSI where no power is transferred to the load. In nonshoot-through state, power is transferred from dc source to ac load, which is similar to the active state of the multilevel VSI. However, the use of more number of high-power passive reactive elements in the intermediate

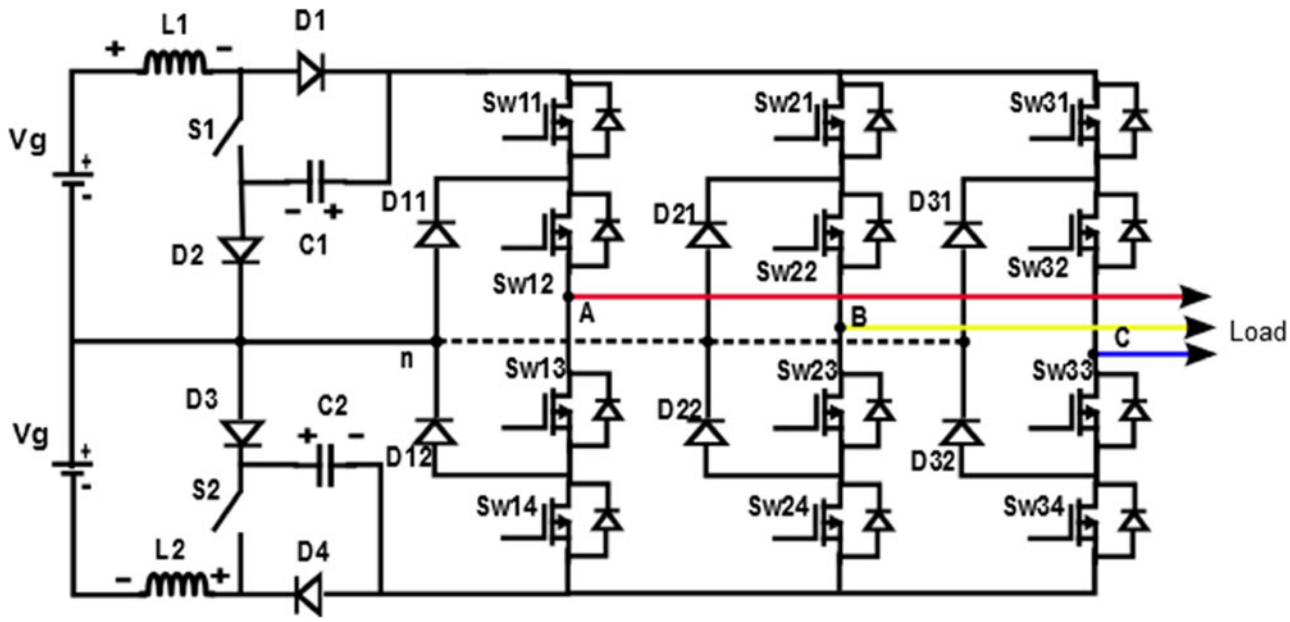


Fig. 1. Circuit diagram of a three-level *LC*-switching voltage boost NPC inverter.

network as well as isolated dc power supply increases the system size, weight, and cost. In literature [16], [17], a single *LC* impedance network-based three-level ZSI is discussed which uses less number of high-power passive components (two capacitors and two inductors) and single split-dc source, but in this multilevel inverter, the voltage rating of the capacitor is nearly double than the conventional three-level Z-source NPC inverter. The source/input current of the three-level NPC ZSI is discontinuous in nature which may increase the stress on source and is not desirable in some of the application like fuel cell, ups system, HEV, etc., [18], [19]. Multilevel quasi-Z-source inverter (QZSI) is an improved derivative of a multilevel ZSI [20], where the source current is continuous in nature and voltage stress across the inverter switches are comparatively less. Cascaded quasi-Z-source multilevel inverter uses two or more isolated dc sources and more number of high-power passive reactive elements for better quality single-stage power conversion as discussed in [21]–[23]. Similarly, a three-level NPC QZSI is discussed in [24], where a quasi-Z-source network is incorporated with conventional NPC structure to give multilevel output. However, the use of more number of high-power passive reactive elements and multiple isolated dc power supply in multilevel QZSI [20]–[22] increases the system size, cost, as well as weight. In this paper, a three-level *LC*-switching-based voltage boost NPC inverter is proposed for boosting the input voltage and give required three-level ac output voltage in a single stage. It uses comparatively less number of passive reactive elements (only two inductors and two capacitors), two active switches, and four diodes in the intermediate network between dc source and inverter leg at the same time it provides all the advantages of multilevel QZSI. As a result, system size and weight are reduced. Though the cost of extra switches and diodes are not much less than the extra passive components (inductors and capacitors) used in multilevel QZSI but can be used in low-power or medium-power applications where size and weight are main constraints. Rest of this paper is organized as follows. Operation of the proposed converter with different operating modes and mathematical validation is presented in Section II. A pulse width modulation (PWM) technique is discussed in Section III, experimental and simulation results are discussed in Section IV, and the paper is ended with a conclusion in Section V.

II. Three-Level *LC*-Switching-Based Voltage Boost NPC Inverter

Fig. 1 shows the schematic diagram of a three-level *LC*-switching-based voltage boost NPC inverter, which is able to boost the input dc voltage source ("V_g") and give required three-level ac voltage unlike conventional NPC VSI. Here, the input source can be either two equal dc sources or single split dc source. This single split dc can be created by feeding a dc source parallel to two series-connected capacitors, where the interconnection point between these capacitors can be taken as neutral point [26]. The intermediate network between dc source and inverter leg is comprised of two inductors (L_1, L_2), two capacitors (C_1, C_2), two active switches (S_1, S_2), and four diodes (D_1, D_2, D_3, and D_4). Whereas a conventional three-level Z-source NPC inverter uses four inductors, four capacitors, and two diodes in the intermediate network between inverter leg and input dc as discussed in the literature [14], [15]. In these conventional Z-source NPC inverters, diodes are connected in series with the input dc source to boost the voltage and the input current is discontinuous in nature. In [24], the NPC QZSI is discussed, where the input current is continuous in nature, but it uses equal values of four inductors, four capacitors, and two diodes in the intermediate network as discussed in Section I. The proposed inverter, however, uses half of the number of passive components (two inductors and two capacitors) in the intermediate network by utilizing extra two switches (S_1 and S_2) and two diodes at the same time maintains all the advan-

TABLE I
SWITCHING STATE AND SWITCHING COMBINATION OF AN *LC*-SWITCHING BOOST NPC INVERTER ($x = 1, 2, 3$)

State of Operation	ON Switches	Voltage
Nonshoot-through state	S_{wx1}, S_{wx2}	$+V_{dc}$
Nonshoot-through state	S_{wx3}, S_{wx4}	$-V_{dc}$
Shoot-through state	S1, S2, $S_{wx1}, S_{wx2}, S_{wx3}, S_{wx4}$	0
Zero state	S_{wx2}, S_{wx3}	0

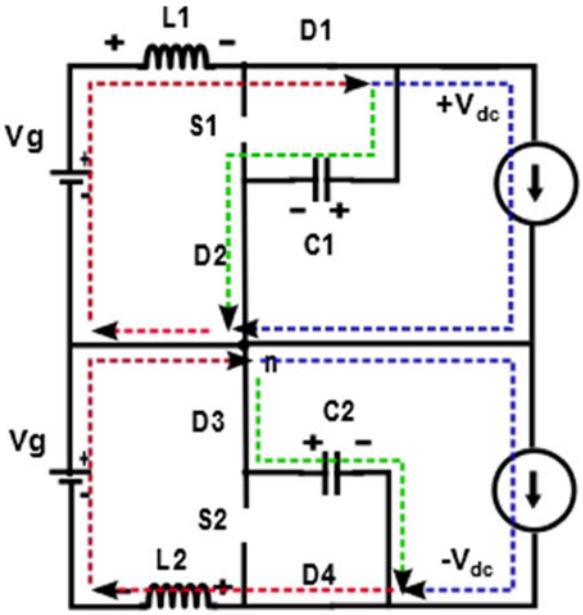


Fig. 2. Equivalent circuit during nonshoot-through state operation of an *LC*-switching boost NPC inverter.

tages of NPC QZSI. As a result, the proposed inverter can be useful in the applications where size and weight are main constraints. Traditional NPC three-level VSI is basically operated in two states, i.e., active state (or nonshoot-through state) and zero state to give three distinct voltage levels (i.e., $+V_{dc}$, 0, $-V_{dc}$). Whereas the proposed inverter uses additional one more state, i.e., shoot-through state to boost the input dc voltage and give three distinct voltage levels ($+V_{dc}$, 0, $-V_{dc}$) in a single stage. The detailed switching pattern at each state is summarized in Table I. The possible modes of operation of the proposed inverter are discussed as below.

A. During Nonshoot-Through State (or Active State)

It is similar to the active state of conventional NPC VSI where power is transferred from dc source to ac load. In this interval of operation, the ac load attains either "$+V_{dc}$" or "$-V_{dc}$" voltage level across ac load with respect to neutral point "*n*." The switches S_{wx1} and S_{wx2} (where $x = 1, 2, 3$) are switched "ON" and switch "S_1" is switched "OFF" to achieve "$+V_{dc}$" across ac load with respect to neutral point "*n*," which in turn forward biases the diodes "D_1" and "D_2." As a result, both source "V_g" and inductor "L_1" energize the capacitor "C_1" as well as supply power to the load, as shown in Fig. 2. Similarly,

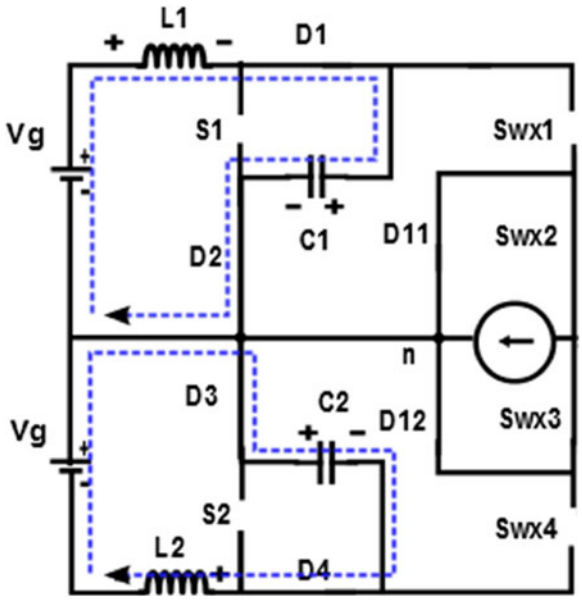


Fig. 3. Equivalent circuit during zero-state operation of an *LC*-switching boost NPC inverter.

the switches S_{wx3} and S_{wx4} are switched "ON" and switch "S2" is switched "OFF" to achieve "$-V_{dc}$" across ac load with respect to neutral point "*n*," which in turn forward biases the diodes "D_3" and "D_4." As a result, both source "V_g" and inductor "L_2" energize the capacitor "C_2" as well as supply power to the load, as shown in Fig. 2. Here, for easy understanding, the load has been represented by current source as for small duration the load current is assumed to be constant.

B. During Zero State

In this state, no power is transferred to ac load from dc source similar to the zero state of conventional NPC VSI. The switches S_{wx2} and S_{wx3} are switched "ON" and switches "S_1," "S_2," "S_{wx1}," and "S_{wx4}" are switched "OFF" to achieve "0" voltage across load, which in turn forward biases the diodes "D_1," "D_2," "D_3," and "D_4." As a result, upper source "V_g" and inductor "L_1" energize the capacitor "C_1" as well as lower source "V_g" and inductor "L_2" energize the capacitor "C_2," as shown in Fig. 3.

C. During Shoot-Through State

During this mode of operation, the switches "S_1" and "S_2" and all the switches of one or more inverter legs are turned "ON," which in turn reverse biases the diodes "D_1," "D_2," "D_3," and "D_4." As a result, upper dc voltage source "V_g" and capacitor "C_1" energize the inductor "L_1." At the same time, lower dc voltage source "V_g" and capacitor "C_2" energize the inductor "L_2," as shown in Fig. 4. Shoot-though state is placed inside the conventional zero state, without interfering the nonshoot-through state (i.e., active state). In nonshoot-through state and zero state ($(1-D)\ T_s$), the voltage across inductors "L_1" and

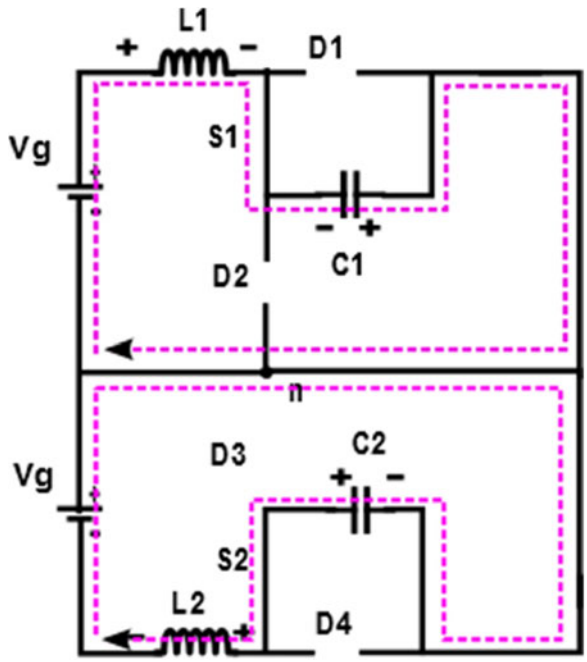


Fig. 4. Equivalent circuit during shoot-through state operation of an *LC*-switching boost NPC inverter.

"L_2" are found to be (from Figs. 2 and 3)

$$V_{L1} = V_g - V_{C1} \tag{1}$$

$$V_{L2} = V_g - V_{C2}. \tag{2}$$

Similarly, currents through the capacitors "C_1" and "C_2" are found to be

$$i_{C1} = i_{L1} - i_{\rm ac} \tag{3}$$

$$i_{C2} = i_{L2} - i_{\rm ac}. \tag{4}$$

During shoot-through state (DT_s), the voltages across inductors "L_1" and "L_2" are found to be (from Fig. 4)

$$V_{L1} = V_g + V_{C1} \tag{5}$$

$$V_{L2} = V_g + V_{C2}. \tag{6}$$

The currents through the capacitors "C_1" and "C_2" are found to be

$$i_{C1} = -i_{L1} \tag{7}$$

$$i_{C2} = -i_{L2}. \tag{8}$$

Applying volt–second balance in steady-state equilibrium across the inductors "L_1" and "L_2", respectively, [21]

$$(V_g - V_{C1})(1 - D) + (V_g + V_{C1})D = 0 \tag{9}$$

$$(V_g - V_{C2})(1 - D) + (V_g + V_{C2})D = 0. \tag{10}$$

Solving (9) and (10), the voltage gains at capacitors "C_1" and "C_2" are found to be

$$V_{C1} = V_{C2} = \frac{V_g}{(1 - 2D)}. \tag{11}$$

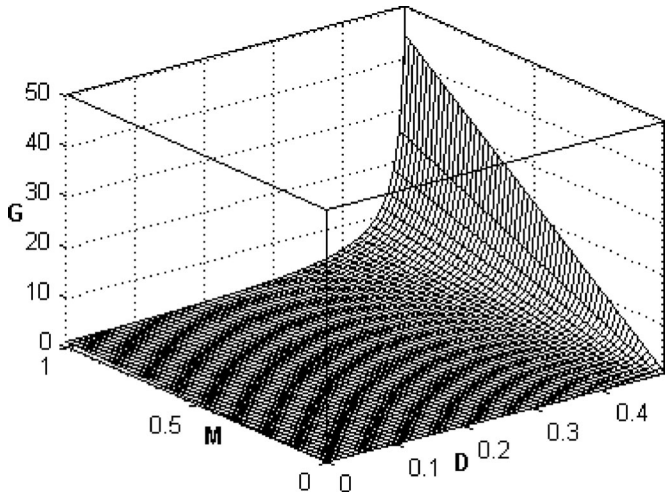


Fig. 5. Relationship plot of voltage gain factor (*G*) versus shoot-through duty ratio (*D*) versus modulation index (*M*).

Applying charge-second balance in steady-state equilibrium across the capacitors "C_1" and "C_2", respectively, [21]

$$(i_{L1} - i_{\rm ac})(1 - D) - Di_{L1} = 0 \tag{12}$$

$$(i_{L2} - i_{\rm ac})(1 - D) - Di_{L2} = 0. \tag{13}$$

Solving (12) and (13), the input current is found to be

$$I_i = I_{L1} = I_{L2} = \frac{(1 - D)i_{\rm ac}}{(1 - 2D)}. \tag{14}$$

From the equivalent circuit (see Fig. 2), it can be observed that the dc voltage fed to the inverter leg "$V_{\rm dc}$" during active state (i.e., nonshoot-through state) is equal to the capacitor voltages. The peak output ac phase voltage is found to be

$$V_m = MV_{\rm dc} = \frac{MV_g}{(1 - 2D)}. \tag{15}$$

The boost factor of the converter is found to be

$$B = \frac{1}{(1 - 2D)}. \tag{16}$$

The voltage gain factor (*G*) of the inverter can be expressed as

$$G = \frac{M}{(1 - 2D)}. \tag{17}$$

The relationship between voltage gain factor (*G*), shoot-through duty ratio (*D*), and modulation index (*M*) is presented in a 3-D surface plot, as shown in Fig. 5. From this relationship plot as well as (15), it is observed that the *LC*-switching boost NPC inverter can be operated as a buck–boost converter by choosing suitable values of *M* and *D* to get required output ac load voltage. From (11), it can be noticed that the converter cannot be operated with shoot-through duty ratio (*D*) more than 0.5 similar to ZSI. For ensuring shoot-through state not to overlap nonshoot-through state (or active state) in any switching cycle, the shoot-through period can be taken maximum up to

zero state, i.e.,

$$M + D \leq 1. \tag{18}$$

Under continuous-conduction mode of operation, the inductors current ripple (Δi_{L1} and Δi_{L2}) and capacitors voltage ripple (ΔV_{C1} and ΔV_{C2}) of the inverter can be expressed as

$$\Delta i_{L1} = \frac{V_g + V_{C1}}{L_1} DTs \tag{19}$$

$$\Delta i_{L2} = \frac{V_g + V_{C2}}{L_2} DTs \tag{20}$$

$$\Delta V_{C1} = \frac{I_{L1}}{C_1} DTs \tag{21}$$

$$\Delta V_{C2} = \frac{I_{L2}}{C_2} DTs. \tag{22}$$

From the above relationships, it is observed that based on the allowable inductor current ripple or input current ripple for different applications, suitable values of inductors (L_1 and L_2) can be used. Similarly based on allowable dc-link voltage ripple for different applications suitable values of capacitors (C_1 and C_2) can be used. By increasing switching frequency also values of these passive components can also be optimized further.

III. PWM Control of an *LC*-Switching Boost NPC Inverter

The gate control signal for the inverter leg switches is generated using a unipolar PWM technique in each phase for eliminating first center band harmonics as well as to achieve three-level pole voltages [25]. Here, for each phase, two modulating sine waves of 180° phase displacement ($V_a(t)$ and $-V_a(t)$) are compared with high-frequency triangular carrier signal ($V_{\rm tri}(t)$), as shown in Fig. 6. For three phases, these modulating signals ($V_a(t)$ and $-V_a(t)$) are phase displaced by 120° and compared with triangular carrier signal to generate gate control signal for the inverter leg switches. The shoot-through gate signal is generated by comparing two fixed reference signals ($V_{\rm st}$ and $-V_{\rm st}$) with the carrier signal ($V_{\rm tri}(t)$). The voltage gain factor (G) decides the amplitude of fixed signals ($V_{\rm st}$ and $-V_{\rm st}$) as well as modulating signals ($V_a(t)$ and $-V_a(t)$). For ensuring shoot-through state not to impede active state (or nonshoot-through state), shoot-through state is placed within the zero state in each switching cycle, as shown in Fig. 6. To ensure voltage balance across the capacitors, a shoot-through offset is added by using the control logic presented in [28]. The shoot-through gate signal is fed to the switches in the intermediate network ("S_1" and "S_2"). Whereas gate signal fed to the inverter leg switches are the combination of shoot-through signal as well as signal generated from the comparison of modulating signals and carrier signal.

IV. Simulation and Experimental Results

The proposed inverter has been analyzed and verified by performing simulation in MATLAB Simulink as well as experiment. The experimental validation has been done by developing

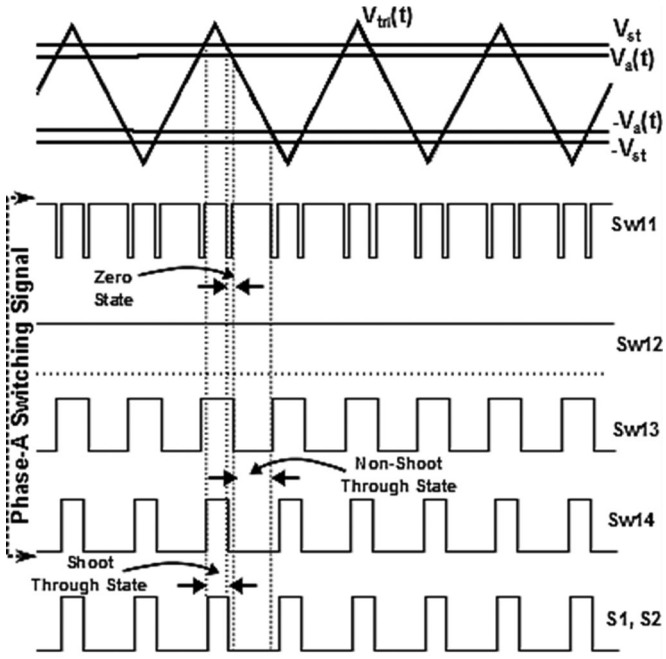


Fig. 6. PWM control of an *LC*-switching voltage boost NPC inverter.

TABLE II
Parameters Used in the Experiment

Parameter	Attributes
Input voltage (V_g)	48 V
Inductor (L_1)	6 mH
Inductor (L_2)	6 mH
Capacitor (C_1)	2000 μF
Capacitor (C_2)	2000 μF
AC output phase voltage ($V_{\rm ph}$)	110 V (rms), 50 Hz
Carrier frequency (f_s)	2.5 kHz
Modulating signal frequency (f_m)	50 Hz
Load (Z_l) per phase	160 Ω

a laboratory prototype. The circuit parameters have been taken for simulation and are shown in Table II. The *LC*-switching boost NPC multilevel inverter has been simulated to achieve phase voltage ($V_{\rm ph}$) of 110 V (rams) from 48-V input dc supply (V_g). Using (15) and (18), for the above desired phase voltage, shoot-through duty ratio (D) as well as modulation index (M) have been found to be 0.4091 and 0.5909, respectively. Carrier frequency (f_s) of 2.5 kHz has been used to generate PWM gate signal fed to the switches. Modulating signal frequency has been taken same as the frequency of the required output ac voltage. Performing simulation, the voltage developed across both the capacitors "C_1" and "C_2" has been found to be the same as theoretical values (using (11)), i.e., $V_{C1} = V_{C2} \approx 260$ V with negligible ripple, as shown in Fig. 7(c) and (d). Similarly, the input current (i_L) for the load 160 Ω has been found to be same as estimated values (calculated using (14)), i.e., $i_L \approx 6$ A, as shown in Fig. 7(b). A three-level pole voltage ($V_{\rm an}$) has been observed with amplitude +260, 0, −260 V, as shown in Fig. 8(d). Similarly, phase voltage ($V_{\rm ph}$), phase current ($I_{\rm poh}$),

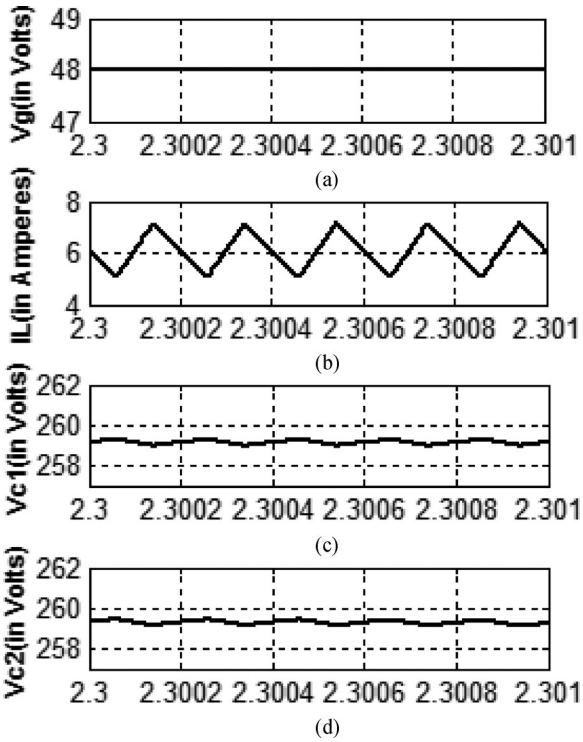


Fig. 7. (a) Input dc voltage (V_g) in volts versus time in seconds. (b) Input current (I_L) in amperes versus time in seconds. (c) Voltage developed across capacitor C_1 (V_{c1}) in volts versus time in seconds. (d) Voltage developed across capacitor C_2 (V_{c2}) in volts versus time in seconds of an *LC*-switching voltage boost NPC inverter.

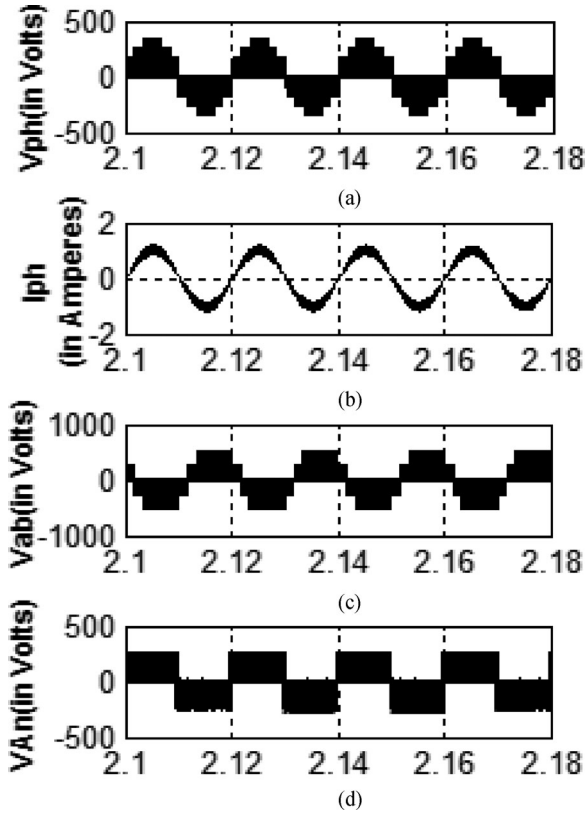


Fig. 8. (a) Phase voltage ($V_{\rm ph}$) in volts versus time in seconds. (b) Phase current ($I_{\rm poh}$) in amperes versus time in seconds. (c) Line-line voltage ($V_{\rm ab}$) in volts versus time in seconds. (d) Pole voltage ($V_{\rm an}$) in volts versus time in seconds at three-phase load of an *LC*-switching voltage boost NPC inverter.

and line voltage ($V_{\rm ab}$) have been observed to be same as theoretical value as shown in Fig. 8(a)–(c), respectively. The total harmonic distortion (THD) of the phase voltage for the above load condition has been found to be nearly 28.71%, as shown in Fig. 9.

For experimental validation, a laboratory prototype has been developed for 48-V dc input (V_g) and 110 V (rms) output phase voltage ($V_{\rm ph}$), as shown in Fig. 10. A 220-W load has been connected to the inverter. Inductors and capacitors have been chosen same as taken in simulation. PWM signals have been generated using field-programmable gate array (FPGA)-based programming in Xilinx Board (Spartan-6 XC6SLX9). TLP250 and SN5401 ICs have been used as gate driver circuit and buffer circuit, respectively. To achieve the above required phase voltage, shoot-through duty ratio (D) and modulation index have been taken same as simulation, i.e., 0.4091 and 0.5909, respectively. From Fig. 11(b), it can be noticed that the voltage across the capacitors has been boosted to 253 V, which is nearly 5.5 times the input dc voltage ($V_g = 48$ V). At the same time, it is also observed that the voltage across both the capacitors is balanced. The voltage developed across the two capacitors is same as the voltage developed capacitors of NPC QZSI for the same "D" and "M." The voltage ripple of capacitors voltages can be controlled with suitable value of capacitors (C_1 and "C_2"). Here, capacitors have been designed for negligible voltage ripple (<0.01%). The input voltage and current waveforms are shown in Fig. 11(a). It can be noticed that the average input current is nine times the load current (i.e., rams current per phase). The input current of

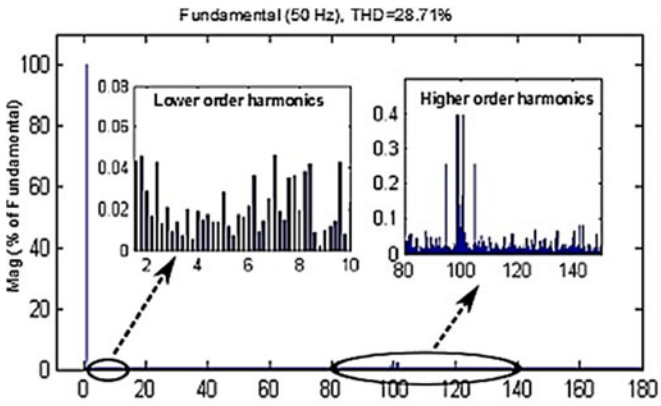


Fig. 9. Harmonic spectrum of an *LC*-switching boost NPC inverter phase voltage ($V_{\rm ph}$).

the multilevel ZSI is discontinuous, whereas it is continuous in the proposed inverter and using (19), (20), its ripple content can be controlled with the suitable value of inductors "L_1"and "L_2". Here, inductors have been designed for 66% peak-to-peak current ripple. This ripple content of the inductor current has been chosen to observe the performance of the proposed inverter in one of the extreme cases like allowing nearly maximum ripple current through the inductors at the same time maintaining negligible voltage ripple across the capacitors. The performance of the inverter will be better by taking lower inductor current

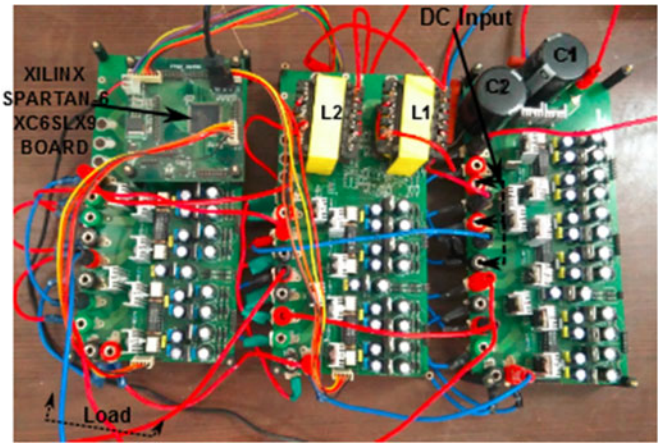
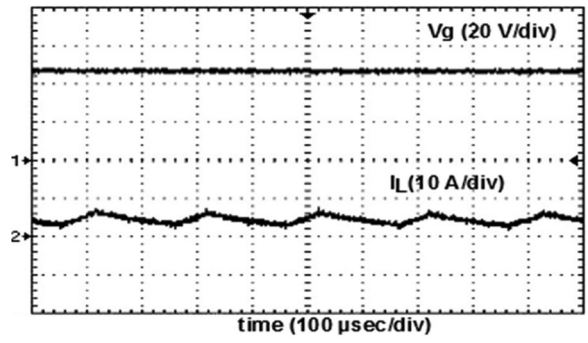
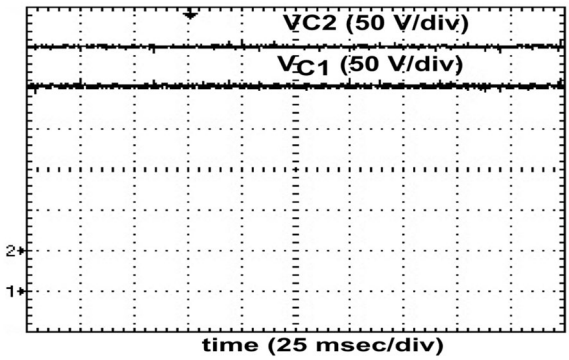


Fig. 10. Laboratory prototype of an *LC*-switching voltage boost NPC inverter.



(a)



(b)

Fig. 11. Experimental results of an *LC*-switching boost NPC inverter. (a) Input voltage (V_g) and input current (I_L). (b) Boost voltage across capacitors (V_{C1} and V_{C2}).

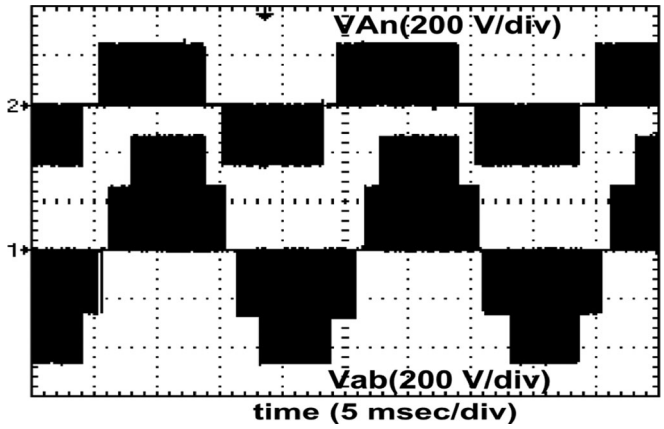


Fig. 12. Experimental waveform of pole voltage ($V_{\rm An}$) and line-line voltage ($V_{\rm ab}$).

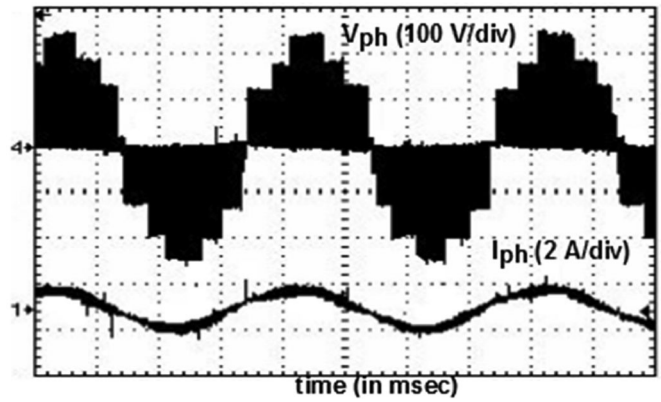


Fig. 13. Experimental results of phase voltage ($V_{\rm ph}$) and phase current ($I_{\rm poh}$).

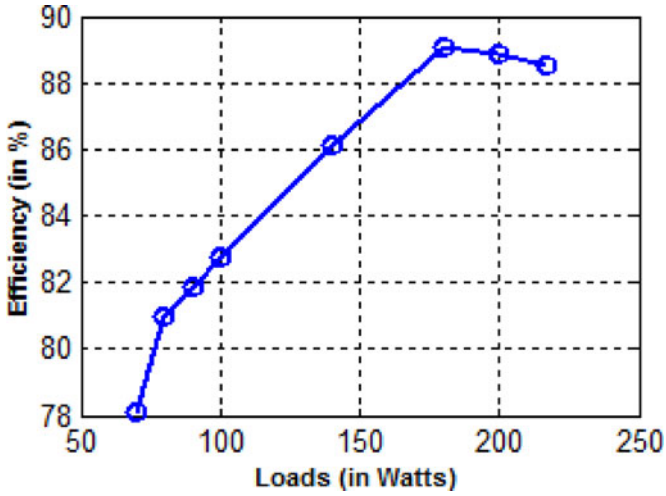


Fig. 14. Efficiency versus load curve of an *LC*-switching boost NPC inverter.

ripple into consideration at the same time relaxing on capacitor voltage ripple based on the allowable ripple content for different applications. The three-level pole voltage ($V_{\rm an}$) (i.e., +253, 0, −253 V) has been observed, as shown in Fig. 12. The line-to-line voltage has been found to be 1.73 times the pole voltage, i.e., $V_{\rm A} = 440$ V, as shown in Fig. 12. Due to the associated no idealities, it can be realized that the voltage amplitudes of experimental results are less than the theoretical values. The experimental phase voltage and phase current are as shown in Fig. 13. The peak value of the phase voltage (V_m) has been observed to be 156 V (i.e., 110-V rams) which is 3.25 times the input dc voltage (V_g). The THD of the phase voltage has been found to be 29.71%. The efficiency of the *LC*-switching boost NPC inverter has been found nearly equal to 89%, as shown in Fig. 14. Whereas the maximum efficiencies of NPC QZSI [24], cascaded [21], and the inverter presented in [27] have been found to be nearly 91%, 85%, and 84.9%, respectively. The efficiency of the proposed inverter is little low because of additional switches and diodes which introduces switching losses, but the use of

less number of passive elements in the inverter reduces system volume and weight.

V. Conclusion

In this paper, a three-level *LC*-Switching voltage boost NPC inverter was presented. The proposed inverter is able to boost the input dc voltage and give required three-level ac output in a single stage unlike conventional NPC VSI. It utilizes the shoot-through state for boosting up the voltage. In comparison to three-level conventional NPC ZSI and NPC QZSI, the *LC*-switching boost inverter uses single split dc source as well as less number of high-power passive reactive elements which results weight and size reduction. In addition to these advantages, the continuous input current of the proposed inverter makes it suitable for the applications like fuel cells, UPS system, PV system, etc. The steady-state operation of the inverter is discussed and voltage gain function is derived. PWM control strategy used for the switching as well as restriction on modulation index and shoot-through duty ratio is also presented. The simulation has been carried out using MATLAB Simulink along with experimental analysis has been done by developing laboratory prototype to verify the proposed inverter.

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