

# Design and Implementation of a Novel Multilevel DC-AC Inverter

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**Abstract** –In this paper, a novel multilevel DC-AC inverter is proposed. The proposed multilevel inverter generates seven levels AC output voltage with the appropriate gate signals design. Also, the low pass filter is used to reduce the total harmonic distortion of the sinusoidal output voltage. The switching losses and the voltage stress of power devices can be reduced in the proposed multi-level inverter. The operating principles of the proposed inverter and the voltage balancing method of input capacitors are discussed. Finally, a laboratory prototype multilevel inverter with 400 V input voltage and output  $220 V_{rms} / 2 \text{ kW}$  is implemented. The multilevel inverter is controlled with sinusoidal pulse-width modulation (SPWM) by TMS320LF2407 digital signal processor (DSP). Experimental results show that the maximum efficiency is 96.9% and the full load efficiency is 94.6%.

**Index Terms**- multilevel, DC to AC inverter, DSP, MPPT

## I. INTRODUCTION

As a result of high technology development, the demand and the quality of electric power is higher than before. Because of the advancement of semiconductor, the specification of power device and power conversion technique is promoted. One of the power converter which can transform DC to AC is called inverter. Inverter is the intermedium which transmit power to other electrical equipment such as uninterruptible power supply, servo motor, air-conditioning system, and smart grid compose of renewable energy shown in Fig. 1. To satisfy different demands and characteristic of loads, the output frequency and voltage have to change with different loads [1]-[3].

In recent years, the amount of power equipment is increasing. Therefore, the harmonic pollution of power system become more serious. Several standards and regulations have been formulated to limit quality of harmonics and power factor of electric equipment such as IEEE Std. 1547 and UL 1741, etc. [4]-[6]. Furthermore, the industry demand higher power applications, the specification of power device is higher. Although IGBT has features of high power rating and high voltage stress, it cannot operate at high frequency. And the design of IGBT gate driver is complicated. MOSFET is the appropriate component to operate at high frequency, but power rating is not as good as IGBT. To solve the problem, many different topology of multilevel use low rating component at high power application.

The purpose of multilevel topology is to reduce voltage rating of power switch. Therefore, it usually use at high power application. By combining output voltages in multilevel form, it has advantages of low  $dv/dt$ , low input current distortion, and lower switching frequency. As a result of advantages of multilevel topology, several topologies have emerged in recent years [7], [8].

A novel multilevel inverter is designed and implemented in

this paper. The major feature of the proposed topology is the reduction of power components. The sinusoidal pulse-width modulation (SPWM) is used to control proposed circuit by TMS320LF2407 digital signal processor (DSP).

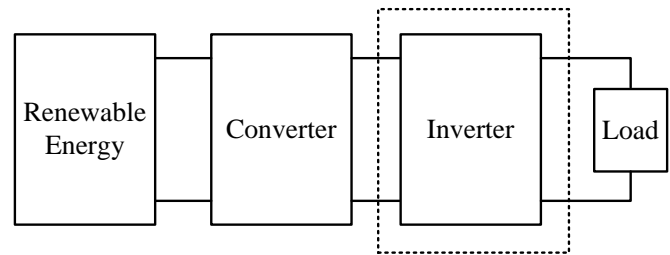


Fig 1. Block diagram of renewable system

## II. POWER STAGE

### A. Circuit Configuration

Fig. 2 shows the proposed novel topology used in the seven-level inverter. An input voltage divider is composed of three series capacitors  $C_1$ ,  $C_2$ , and  $C_3$ . The divided voltage is transmitted to H-bridge by four MOSFET, and four diodes. The voltage is send to output terminal by H-bridge which is formed by four MOSFET. The proposed multilevel inverter generates seven levels AC output voltage with the appropriate gate signals design.

### B. Operating Principles

The required seven voltage output levels ( $\pm 1/3V_{dc}$ ,  $\pm 2/3V_{dc}$ ,  $\pm V_{dc}$ , 0) are generated as follows:

- 1) To generate a voltage level  $V_o = 1/3V_{dc}$ ,  $S_1$  is turned on at the positive half cycle. Energy is provided by the capacitor  $C_1$  and the voltage across H-bridge is  $1/3V_{dc}$ .  $S_5$  and  $S_8$  is turned on and the voltage applied to the load terminals is  $1/3V_{dc}$ . Fig. 3 shows the current path at this mode.
- 2) To generate a voltage level  $V_o = 2/3V_{dc}$ ,  $S_1$  and  $S_4$  are turned on. Energy is provided by the capacitor  $C_1$  and  $C_2$ . The voltage across H-bridge is  $2/3V_{dc}$ .  $S_5$  and  $S_8$  is turned on and the voltage applied to the load terminals is  $2/3V_{dc}$ . Fig. 4 shows the current path at this mode.
- 3) To generate a voltage level  $V_o = V_{dc}$ ,  $S_1$  and  $S_2$  are turned on. Energy is provided by the capacitor  $C_1$ ,  $C_2$ , and  $C_3$ . The voltage across H-bridge is  $V_{dc}$ .  $S_5$  and  $S_8$  is turned on and the voltage applied to the load terminals is  $V_{dc}$ . Fig. 5 shows the current path at this mode.
- 4) To generate a voltage level  $V_o = -1/3V_{dc}$ ,  $S_2$  is turned on at the negative half cycle. Energy is provided by the capacitor  $C_3$  and the voltage across H-bridge is  $1/3V_{dc}$ .  $S_6$

and  $S_7$  is turned on and the voltage applied to the load terminals is  $-1/3V_{dc}$ . Fig. 6 shows the current path at this mode.

- 5) To generate a voltage level  $V_o = -2/3V_{dc}$ ,  $S_2$  and  $S_3$  are turned on. Energy is provided by the capacitor  $C_2$  and  $C_3$ . The voltage across H-bridge is  $2/3V_{dc}$ .  $S_6$  and  $S_7$  is turned on, the voltage applied to the load terminals is  $-2/3V_{dc}$ . Fig. 7 shows the current path at this mode.
- 6) To generate a voltage level  $V_o = -V_{dc}$ ,  $S_1$  and  $S_2$  are turned on. Energy is provided by the capacitor  $C_1$ ,  $C_2$ , and  $C_3$ , the voltage across H-bridge is  $V_{dc}$ .  $S_6$  and  $S_7$  is turned on, the voltage applied to the load terminals is  $-V_{dc}$ . Fig. 8 shows the current path at this mode.
- 7) To generate a voltage level  $V_o = 0$ ,  $S_5$  and  $S_7$  are turned on. The voltage applied to the load terminals is zero. Fig. 9 shows the current path at this mode.

Table I lists the switching combinations at different output levels.

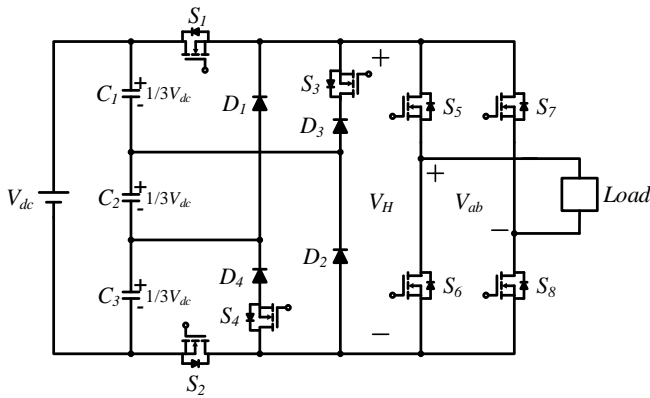


Fig. 2. Proposed seven-level inverter topology.

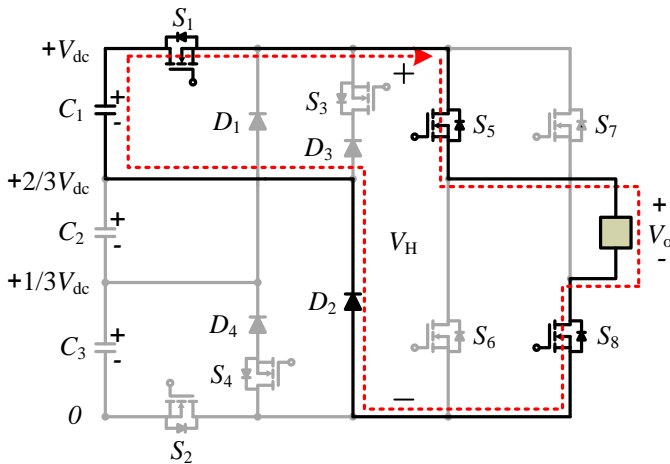


Fig. 3. Switching combination of output voltage level  $1/3V_{dc}$ .

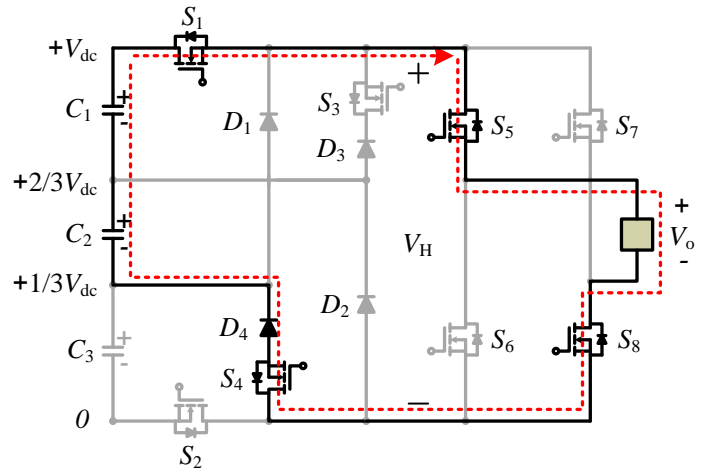


Fig. 4. Switching combination of output voltage level  $2/3V_{dc}$ .

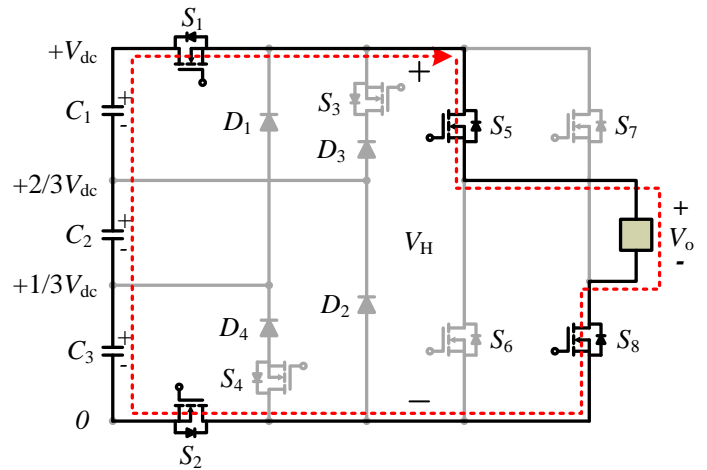


Fig. 5. Switching combination of output voltage level  $V_{dc}$ .

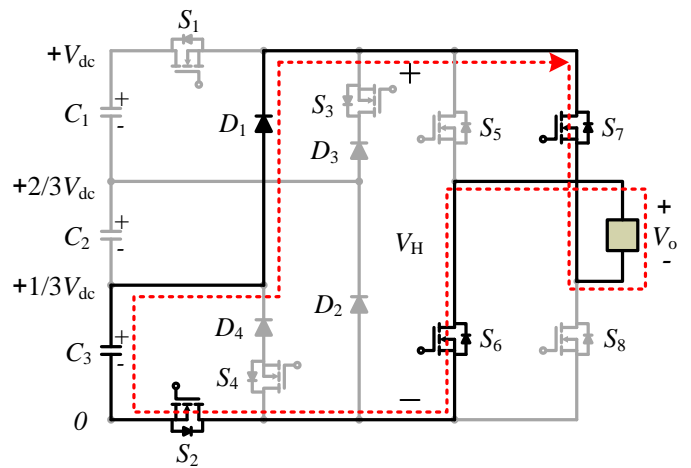


Fig. 6. Switching combination of output voltage level  $-1/3V_{dc}$ .

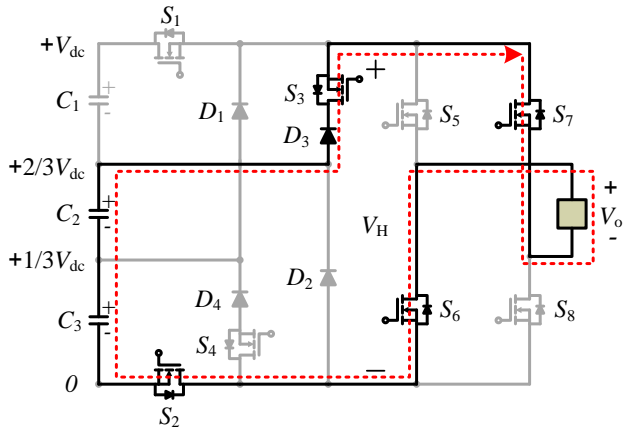


Fig. 7. Switching combination of output voltage level  $-2/3V_{dc}$ .

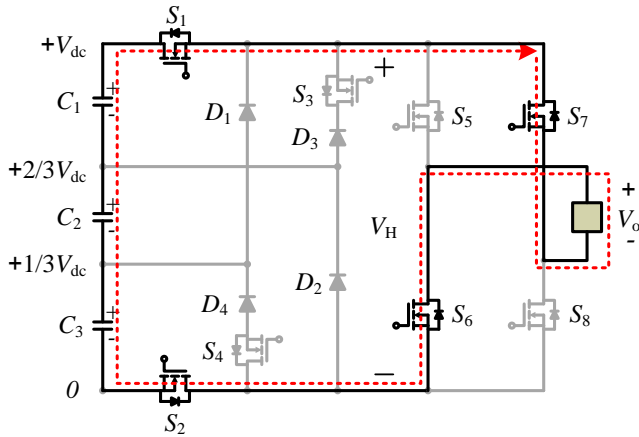


Fig. 8. Switching combination of output voltage level  $-V_{dc}$ .

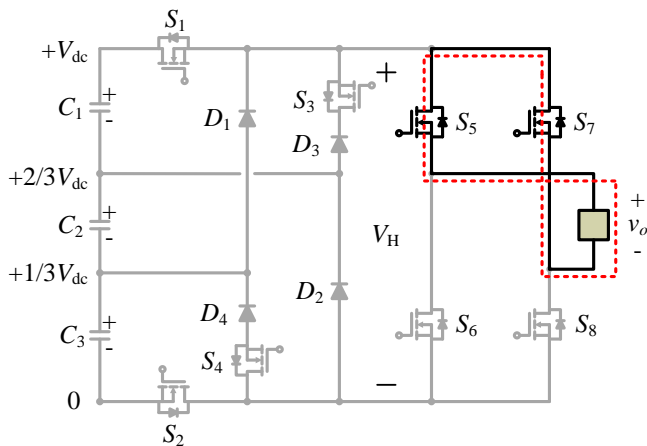


Fig. 9. Switching combination of output voltage level 0.

TABLE I  
SWITCHING COMBINATIONS REQUIRED TO GENERATE THE SEVEN-LEVEL OUTPUT VOLTAGE WAVEFORM

Output voltage $V_o$	Switching combinations							
	$S_1$	$S_2$	$S_3$	$S_4$	$S_5$	$S_6$	$S_7$	$S_8$
$1/3V_{dc}$	on	off	off	off	on	off	off	on
$2/3V_{dc}$	on	off	off	on	on	off	off	on
$V_{dc}$	on	on	off	off	on	off	off	on
$-1/3V_{dc}$	off	on	off	off	off	on	on	off
$-2/3V_{dc}$	off	on	on	off	off	on	on	off
$-V_{dc}$	on	on	off	off	off	on	on	off
0	off	off	off	off	on	off	on	off

### B. Topology Comparison

Table II presents the number of components required to implement a seven-level inverter using the proposed topology and three previously ones [9], [10]: that can be considered as the standard multilevel configurations, the diode-clamped inverter, the capacitor-clamped inverter, and the cascaded multi-cell inverter.

Table II shows that the new topology achieve the reduction in the number of power devices. Table III shows the voltage stress comparison between different type inverters.

TABLE II  
COMPONENTS COMPARISON BETWEEN FOUR DIFFERENT SEVEN-LEVEL INVERTERS

	Proposed	Diode-clamped	Capacitor-Clamped	Cascaded multicell
Input sources	1	1	1	3
Input capacitors	3	6	2	3
Clamped capacitors	0	0	5	0
Power switches	8	12	12	12
Diodes	4	10	0	0

TABLE III  
VOLTAGE STRESS COMPARISON BETWEEN FOUR DIFFERENT SEVEN-LEVEL INVERTERS

	Proposed	Diode-clamped	Capacitor-Clamped	Cascaded multicell
Input sources	$V_o$	$2V_o$	$2V_o$	$V_o/3$
Input capacitors	$V_o/3$	$V_o/3$	$V_o/2$	$V_o/3$
Power switches	$V_o$	$V_o/3$	$V_o/3$	$V_o/3$
Diodes	$2V_o/3$	$3V_o/2$	N/A	N/A

### III. VOLTAGE BALANCING CIRCUIT BASED ON RSCC

Since the voltage deviation causes larger harmonics distortion in the output voltage, voltage balancing circuits are indispensable for the capacitors in the multilevel inverters [11]-[15]. By using resonant switching capacitor converter, the voltage balance of input capacitors is achieved. Fig. 10 shows the circuit configuration of a unit of the RSCC. The duty cycle of every switch is equal to 50%. The voltage of  $C_1$  is higher than the voltage of  $C_2$ . Since the average current of  $C_1$  is higher than that of  $C_2$  at one switching cycle, most of the charges flow from  $C_1$  to  $C_2$ . After few switching cycles, the voltage of  $C_1$  and  $C_2$  are equal. Fig. 11 shows the waveforms of the RSCC.

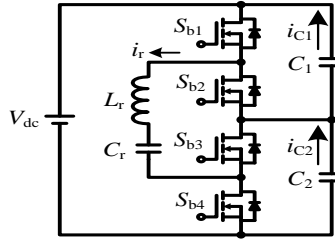


Fig. 10. Circuit configuration of RSCC.

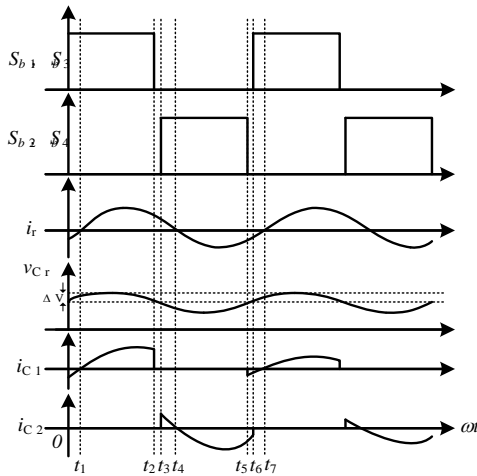


Fig. 11. Waveforms of RSCC.

Fig. 12 shows the configuration of proposed seven-level inverter with RSCC. To apply RSCC at seven-level configuration, two switches  $S_{b5}$  and  $S_{b6}$ , resonant inductor  $L_r$ , and resonant capacitor  $C_r$  are added. In this application, switches  $S_{b1}$ ,  $S_{b3}$ , and  $S_{b5}$  are turned on at the same time;  $S_{b2}$ ,  $S_{b4}$ , and  $S_{b6}$  are turned on at the same time. The duty of each switch is equal to 50%.

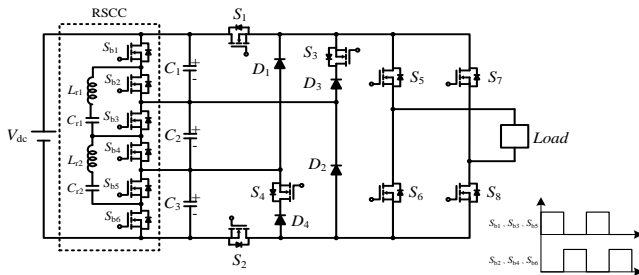


Fig. 12. The proposed multilevel inverter with RSCC.

### IV. APPLICATION OF SPWM

In this paper, several triangular carriers are distributed by phase disposition technique. The advantage of phase disposition technique are uncomplicated to realize and less total harmonic distortion [16], [17]. These carriers compare with a reference sine waveform  $v_{sin}$  to get signal of switches. The peak-to-peak value of triangular carrier is  $V_{tri}$ . The frequency of carrier is switching frequency of inverter. The peak value of reference sine wave is  $\hat{V}_{sin}$ , and the modulation index  $m_A$  is defined as:

$$m_A = \frac{\hat{V}_{sin}}{3 \cdot \hat{V}_{tri}} \quad (1)$$

According to (1), the relationship between the peak value of output sine wave and  $m_A$  can be expressed as:

$$V_o = m_A \cdot V_{dc} \quad (2)$$

Fig. 13 shows the reference sine wave, carriers, and control signals of switches.

The method to determine switch signals in Fig. 12 are as follow:

- (a)  $v_{sin} < 0$  and  $v_{sin} > v_{tri2} \rightarrow S_2$  is turned on
- (b)  $v_{sin} > v_{tri4} \rightarrow S_4$  is turned on
- (c)  $v_{sin} < v_{tri8} \rightarrow S_7$  is turned on
- (d)  $v_{sin} > v_{tri8} \rightarrow S_8$  is turned on
- (e)  $v_{sin} > 0$  and  $v_{sin} < v_{tri1} \rightarrow S_1$  is turned on
- (f)  $v_{sin} < v_{tri3} \rightarrow S_3$  is turned on
- (g)  $v_{sin} > v_{tri6} \rightarrow S_5$  is turned on
- (h)  $v_{sin} < v_{tri6} \rightarrow S_6$  is turned on

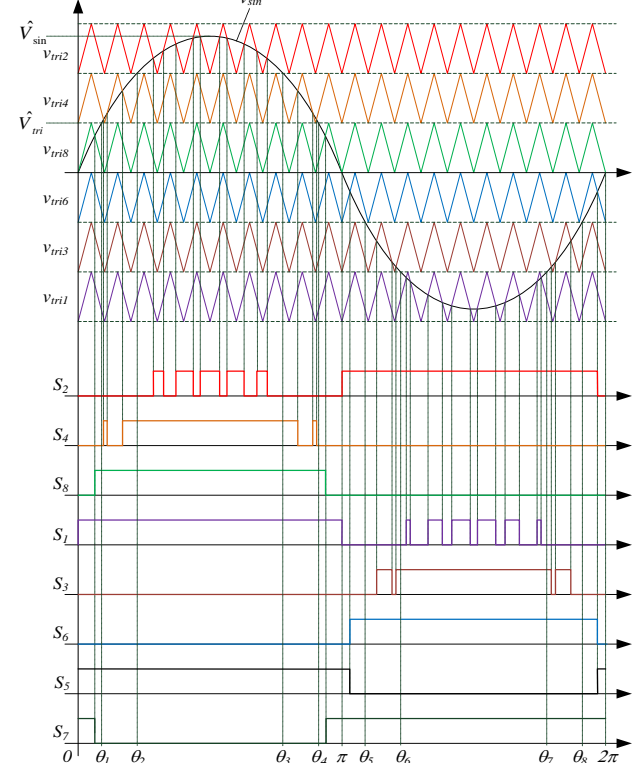


Fig. 13. Reference sine wave, carriers, and control signals of switches.

## V. PI CONTROL USED IN MODIFIED SPWM

Modified SPWM based on PI control is used in this paper [18], [19]. Fig. 14 shows the block diagram of PI control. The block diagram can be expressed in S domain as:

$$u(s) = [K_p + \frac{K_i}{s}]e(s) \quad (11)$$

from (11), the equation can be transformed in Z domain as:

$$u(z) = [K_p + \frac{K_i}{1-z^{-1}}]e(z) \quad (12)$$

then transform (12) become difference equation is express as:

$$u[n] = K_p e[n] + K_i e[n] - K_p e[n-1] + u[n-1] \quad (13)$$

Fig. 15 shows system configuration and control block. System detects output voltage first, and compares this signal with a built-in reference. Then, the system feedbacks an error to PI controller. Finally, the PI controller exports a control signal to gate driver.

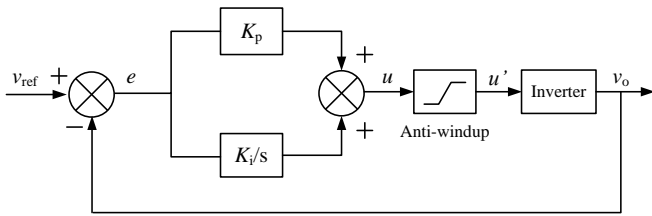


Fig. 14 Block diagram of PI control.

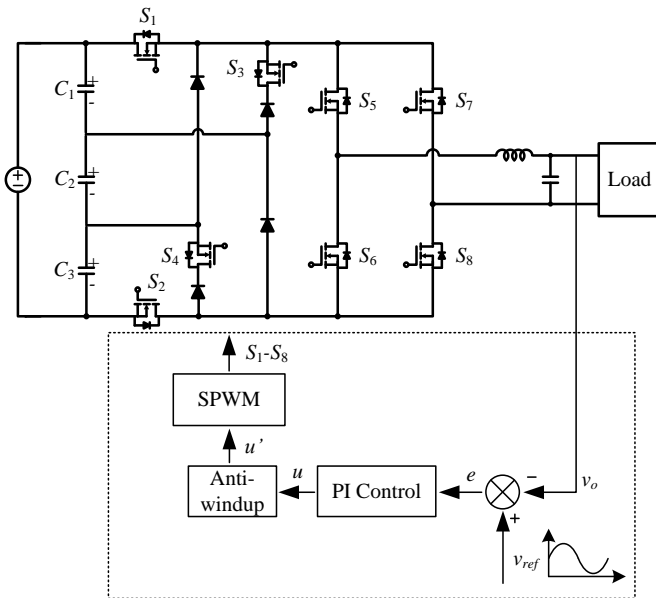


Fig. 15. Seven-level inverter with control algorithm.

The main idea of modified SPWM is to record the previous error of output voltage, and generate a suitable correction at the latest cycle. Because the frequency of carrier is 18 kHz and the frequency of output sine wave is 60 Hz, the number of times of switching is 300 times. Fig. 16 shows schematic of modified SPWM.

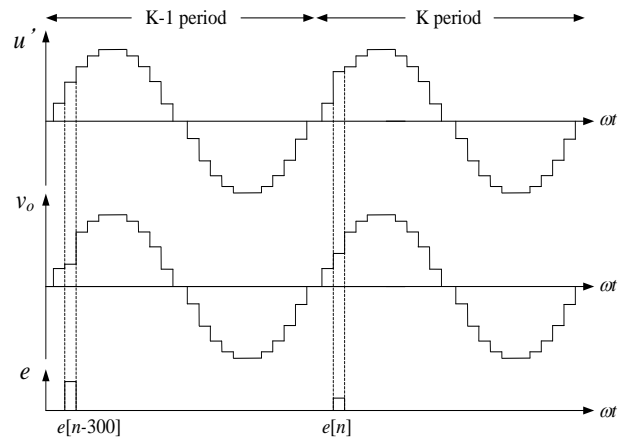


Fig. 16. Schematic of modified SPWM.

$v_{ref}[n]$  is defined as the reference output voltage,  $v_o[n]$  is the feedback of output voltage, and  $e[n]$  is error between reference output and feedback output which is expressed as (14):

$$e[n] = v_{ref}[n] - v_o[n] \quad (14)$$

let  $K_1 = K_p + K_i$ ,  $K_2 = K_p$ , then made  $e[n]$  multiplied by  $K_1$  and  $e[n-300]$  multiplied by  $K_2$ . Then add the previous output signal  $u'[n-300]$ . Finally, it can get the output of PI controller after process by the anti-windup.

$$u'[n] = K_1 \cdot e[n] - K_2 \cdot e[n-300] + u'[n-300] \quad (15)$$

## VI. EXPERIMENT RESULTS

A TMS320LF2407A DSP is used to verify the proposed seven-level inverter. Table IV shows the characteristics of the inverter. Fig. 17 shows the prototype of the seven-level inverter. This prototype consist of detect, gate driver, DSP, RSCC, and seven-level inverter.

TABLE IV  
THE SPECIFICATION OF THE PROPOSED INVERTER

Input voltage $V_{dc}$	400 V
Output voltage $V_o$	220 V <sub>rms</sub>
Rated output power $P_o$	2 kW
Switching frequency $f_s$	18 kHz



Fig. 17. Experimental setup for the prototype.

Fig. 18 presents the output voltage waveform  $v_{ab}$  showing the desired seven voltage levels and output waveform  $v_o$ . The seven voltage levels in the figure are  $\pm 133$  V,  $\pm 267$  V,  $\pm 400$  V, 0 V. Fig. 19 and 20 show the output waveform harmonic spectrum calculated by power analyzer YOKOGAWA WT3000 with a proprietary FFT program, and the high frequency composition is attenuated by LC low pass filter.

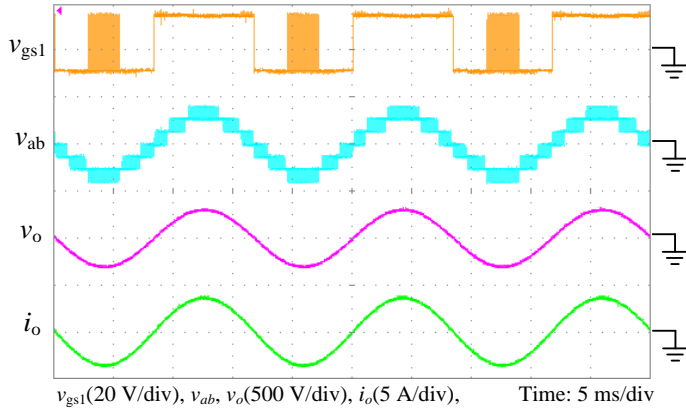


Fig. 18. Waveforms of  $v_{gsl}$ ,  $v_{ab}$ ,  $v_o$ , and  $i_o$  at 500 W

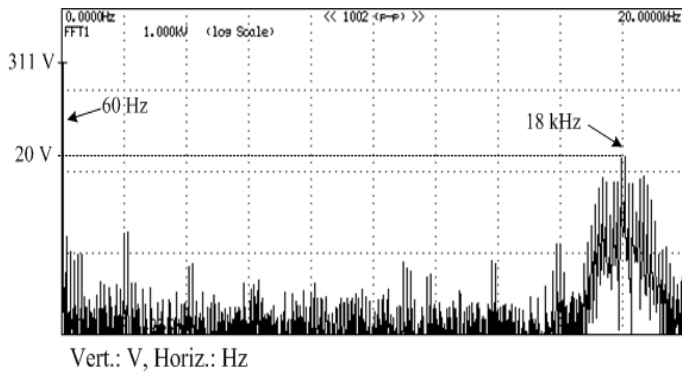


Fig. 19. Output voltage harmonic spectrum of  $v_{ab}$  calculated by FFT.

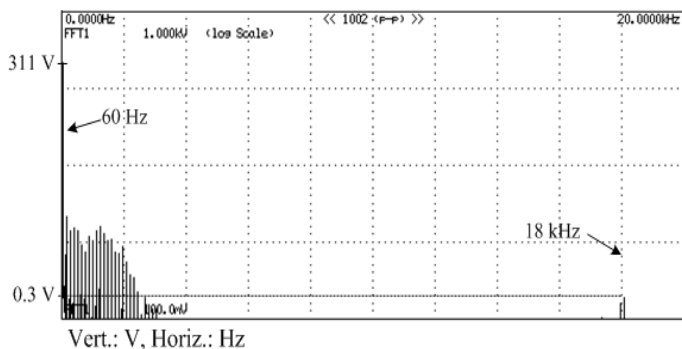


Fig. 20. Output voltage harmonic spectrum of  $v_o$  calculated by FFT.

Fig. 21 shows capacitor voltage  $V_{C2}$ , output voltage  $v_o$ , and output current  $i_o$  at 1000 W. In this figure, the capacitor voltage is 133 V. Thus, the function of voltage balancing is achieved. Fig. 22 shows capacitor voltage  $V_{C2}$ , output voltage  $v_o$ , and output current  $i_o$  at 2000 W. The THD of output voltage is 0.9%.

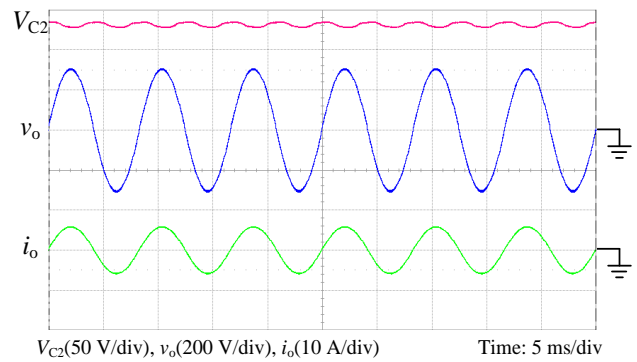


Fig. 21. Waveforms of  $v_{C2}$ ,  $v_o$ , and  $i_o$  at 1000 W

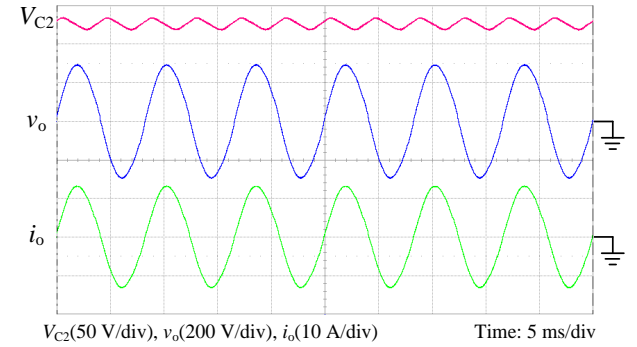


Fig. 22. Waveforms of  $v_{C2}$ ,  $v_o$ , and  $i_o$  at 2000 W

Multilevel structure is usually used in inductive loads such as motor. Thus, this paper applies the proposed topology in inductive load. Fig. 23 shows the test block diagram. The inductor and the resistor are connected in series, and PF is set at 0.95. Fig. 24 shows the output voltage and current at 400 VA. The THD of output voltage is 3.3%.

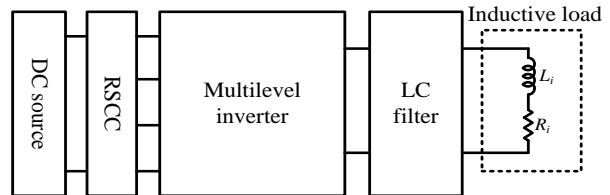


Fig. 23. Test block diagram of inductive load.

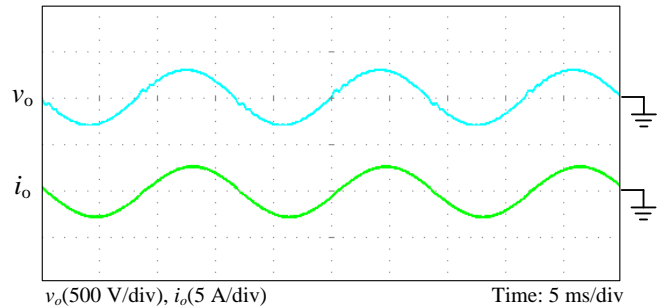


Fig. 24. Waveforms of  $v_o$  and  $i_o$  at 400 VA.

The efficiency at different output power is showed in Fig. 25. The output power is from 200 W to 2000W. The highest efficiency is 96.9% at 800 W, and the lowest is 94.6% at 2000 W. The efficiency is always above 94.5%.



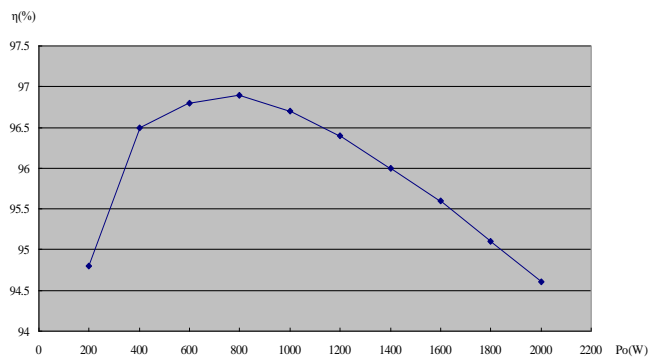


Fig. 25. The efficiency of the proposed inverter.

## VII. CONCLUSION

A novel seven-level inverter is designed and implemented with DSP in this paper. The main idea of the proposed configuration is to reduce the number of power device. The reduction of power device is proved by compare with traditional structures. Finally, a laboratory prototype of seven-level inverter with 400 V input voltage and output 220 V<sub>rms</sub> /2 kW is implemented. Experimental results show that the maximum efficiency is 96.9% and the full load efficiency is 94.6%.

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