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Low Leakage Fully Half-Select-Free Robust SRAM Cells with BTI Reliability Analysis

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***Abstract*—This paper presents two different topologies of 11T SRAM cells with fully half-select-free robust operation for bit-interleaving implementation. The proposed 11T-1 and 11T-2 cells successfully eliminate Read disturb and Write half-select disturb and also improve the Write-ability by using power-cutoff and write '0'/ '1' only techniques. The 11T-1 and 11T-2 cells achieve 1.83x and 1.7x higher write-yield while both achieve approximately 2x higher read-yield as compared with 6T cell (at V_{DD}=0.9V). The proposed 11T-1 cell also shows 13.6% higher mean Write-margin (WM) compared with existing 11T cell. Both the proposed cells successfully eliminate floating node condition encountered in earlier power cut-off cells during write half-select. Monte-Carlo simulation confirms low-voltage operation without any additional peripheral assist circuits. We also present a comparative analysis of Bias Temperature Instability (BTI) reliability impacting the SRAM performance in a predictive 32nm high-k metal gate CMOS technology. Under static stress, the Read Static Noise Margin (RSNM) reduces for all cells. However, 11T-1 and 11T-2 cells improve RSNM by 2.7% and 3.3% under relaxed stress of 10/90. Moreover, the proposed 11T-1 (11T-2) cell improves WM by 7.2% (13.2%), reduces write power by 28.0% (20.4%) and leakage power by 85.7% (86.9%), degrades write delay by 38.1% (23.3%) without affecting read delay/power over a period of 10^8 seconds (approx. 3 years). The 11T-1 (11T-2) cell exhibits 4.8% higher (2% lower) area overhead as compared to earlier 11T cell. Hence, the proposed 11T cells are an excellent choice for reliable SRAM design at nanoscale amidst process variations and transistor aging effect and can also be used in bit-interleaving architecture to achieve multi-cell upset (MCU) immunity.**

***Index Terms*— Static Random Access Memory (SRAM), Bit-Interleaving, Static Noise Margin, Write Margin, Bias Temperature Instability (BTI), Column Half Select (CHS), Multi-Cell Upset (MCU)**

I. INTRODUCTION

WITH the proliferation in the demand of low power devices like wireless sensor networks, implantable biomedical devices and other battery operated portable devices, power dissipation has become a key design constraint. Static Random Access Memory (SRAM) is the major contributor to the power dissipation, as they occupy significant portion of Systems-on-Chip (SoCs), and their portion will grow further in the future [1]. Moreover, with the advent of ultra-scaled technologies, the leakage becomes a serious threat. The power consumption will increase as leakage rises exponentially with reduction in threshold voltage (V_{th}) and gate-oxide thickness [2]. It is, therefore, necessary to minimize the power associated with SRAM in order to have a power efficient design. Reducing the supply voltage is a straight forward way to achieve power efficiency because the active and leakage power reduce quadratically and exponentially respectively with supply voltage [3]. However, at lower supply voltages, process variation severely degrades the performance of SRAM cell [4]. Consequently, Read/Write failure probability is significantly increased in the conventional 6T SRAM due to the difficulty in maintaining the device strength ratio in sub-threshold region [5]. Researchers have proposed many configurations of SRAM cells [6]-[13] to overcome Read failure by using a separate read buffer. These cells improve the read static noise margin (RSNM) by decoupling the read/write path but still suffer from poor write margin (WM) in the subthreshold region. Also, various write-assist techniques have been described in the literature to increase the write margin of the SRAM cell [14]-[20]. Wordline (WL) boosting [14], [15] and negative bitline (NBL) [16] are the commonly used write-assist techniques for improving the write-ability by strengthening the driving capability of the write access transistor. However, these techniques result in area and power penalties. Weakening the strength of the cross-coupled inverter pair is another useful way of write-ability enhancement. It includes power cut-off [17], [18], raising [19] or floating [11], [20] the cell VSS, etc.

Recently, Multi-bit soft error/upset (MCU) has threatened the stability of SRAMs at ultra-scaled technology due to the reduction in effective distance between transistors [21]. Bit-interleaving (BI) architectural technique is an efficient way to deal with this error. However, this technique is applicable to the cells, which exhibit fully half-select (HS) free operation. The straight forward approach to achieve HS free operation is to use cross-point cell selection, where write path consists of two access transistors controlled by different row and column based signals [10]. However, stacked transistors in the write-access path severely degrade the write-ability, which makes it necessary to use WL boosting for both the row-based and column-based Write WL at the expense of dynamic power. The two BI cells 11T [17] and 12T [18] were proposed that eliminate HS disturb again by using cross-point selected series connected access transistors. Nevertheless, these cells improve the Write-ability by using Power Cutoff Write-assist and do not require wordline boosting; they suffer from degradation of floating-1 level of data storing nodes Q or QB in column write

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HS cells. They require an extra Pulse-Width-Controller in the column circuitry to achieve very precise pulse width for word-lines during write operation to retain the data in the column write half-select (CHS) cells. Recently, a BI power gated 9T cell [22] has been proposed to solve the HS issue, however the power cut-off used during the write operation again leads to floating of data at storing nodes Q in row half-select (RHS) cells. Therefore, in this work, we propose two new 11T cells that mitigate the HS issue without using write-back or any other assist techniques and support a BI architecture to improve MCU immunity. The first proposed cell (termed as 11T-1) uses supply-cut-off and write '0' only whereas the second proposed cell (termed as 11T-2) uses ground-cut-off and write '1' only technique for write-ability enhancement. The power cut-off in proposed cells does not lead to floating of data storage nodes in any of the HS cell contrary to the existing 11T [17].

Reliability is one of the biggest challenges for designing SRAMs in deep submicron technologies. Scaling below 32nm node leads to reliability concern characterized by progressive degradation of devices due to aging. Bias temperature instability (BTI) is one of the major reliability issue encountered by devices due to aggressive scaling. Negative bias temperature instability (NBTI), observed primarily in PMOS has been the biggest concern of reliability over the years but with the introduction of high-*k* metal gate and its dependence on charge trapping places the positive bias temperature instability (PBTI) as the major reliability issue in NMOS devices [23]. NBTI and PBTI increase the threshold of the transistor with stress time and consequently, degrade the performance of the circuit. It is, therefore, crucial to analyze the impact of NBTI and PBTI on different SRAM performance metrics. The proposed cells, in this work, have also been analyzed for BTI reliability to see the change in performance metrics such as Read SNM, Write-Margin, Read/Write delay, Read/Write power and leakage power due to aging of transistors.

The rest of this paper is organized as follows. In Section II, proposed cell structures and their operations are discussed. In Section III, BTI mechanism, model and its analysis framework are discussed. Section IV presents the simulation setup, results and comparison of SRAM cells considered in this work. Section V then concludes this paper.

II. PROPOSED SRAM CELLS

A. Proposed 11T-1 Cell

Fig. 1 shows the schematic diagram of the proposed 11T-1 SRAM cell. The cell core consists of cross coupled inverter with the addition of Power cut-off with floating-avoidance assist (PCFA). The transistors MP1 and MP3 in PCFA network internally cut off the supply voltage to weaken the pull-up path and provide contention-free discharge of the storage node to improve the write-ability. Whereas, transistor MP2, driven by row based WL avoids the floating-1 situation in CHS cells. The write access transistors MAL and MAR are controlled by column based WLA and WLB signals. Table-I illustrates the status of the control signals in different modes

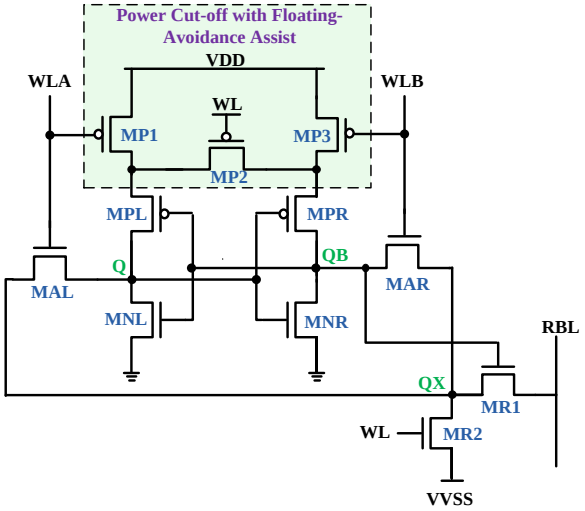

Fig. 1. Proposed 11T-1 cell schematics.

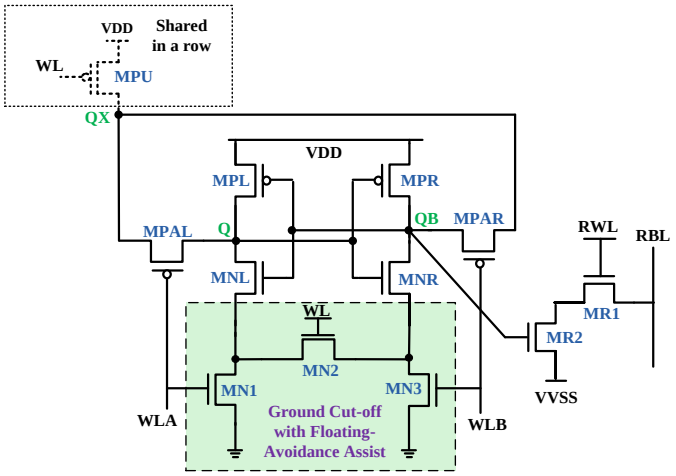

Fig. 2. Proposed 11T-2 cell schematics.

TABLE I
CONTROL SIGNALS DURING VARIOUS MODES OF OPERATION FOR THE PROPOSED 11T-1/11T-2 CELL

Control Signal	Operation			
	Hold	Read	Write '0'	Write '1'
WLA	0/1	0/1	1	0
WLB	0/1	0/1	0	1
WL	0/1	1/0	1/0	1/0
RBL	1	Pre	0/1	1
RWL	0	1	0	0
VVSS	1	0	0/1	0/1

of operation of the proposed cells. During the Write '0' operation, WLA and WL signals are enabled, whereas WLB and VVSS are disabled. The left inverter is completely cut-off from power supply and node Q is easily discharged through transistors MAL and MR2. Similarly for write '1', the WL and WLB are enabled, whereas WLA is disabled. The supply is now cut-off for right inverter and node QB is discharged easily through MAR and MR2 and consequently '1' is written at node Q. The read operation is accomplished by enabling WL signal and keeping WLA and WLB both at '0'. The RBL is pre-charged prior to read operation. The discharging path

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will be on for RBL through transistors MR1 and MR2 depending on the data stored at QB. The disabled WLA and WLB signals enables complete isolation of data storage nodes (Q and QB) from any read disturbing path during the read access. Therefore, the 'read upset' is of no concern even for subthreshold operation. In the Hold Mode, all the control signals are disabled, which provides a completely isolated cross-coupled inverters without any floating node. Therefore, the cell stability in the hold mode is same as 6T cell. The VVSS signal is kept high, which significantly reduces the static power consumption during standby mode.

B. Proposed 11T-2 Cell

Fig. 2 shows the schematic diagram of the proposed 11T-2 SRAM cell. It consists of the similar cell core with the additional Ground-cut-off with floating avoidance assist (GCFA) comprising of MN1, MN2 and MN3. The transistors MN1 and MN3 in GCFA internally cut-off the ground during write-operation and provide contention free charging of high-going node for improving the write-ability. Whereas, transistor MN2, driven by row based WL, prevents the floating-'0' situation in CHS cells. The cell utilizes the single-ended sensing with an additional read buffer comprising of transistors MR1 and MR2. VVSS signal is used to eliminate unnecessary leakage during standby mode. The write access transistors MPAL and MPAR are controlled by column based WLA and WLB signals. Transistor MPU is controlled by row based WL signal, and is shared in a row.

During the Write '0' operation, WLA is enabled, whereas WLB and WL signals are disabled. The right inverter is completely cut-off from ground path and node QB is easily pulled-up through transistors MPAR and MPU without the contention from pull-down transistor MNR. Consequently, Q is discharged to ground through MNL and MN1. The write '1' follows similar procedure due to symmetric write operation.

C. Write-Half-select Operation of Cells

Half-Select disturb is the disturbance caused in storage node of any of the unselected cells in selected rows or column during write operation. HS free operation is necessary for the SRAM cell to be implemented in BI architecture, which is used to solve multi-bit errors. In BI technique, only one bit of a word is placed at a particular location rather than all the bits of a word together. Thus, even when, data upset occurs at multiple bits locally, it is equivalent to single bit-error in different words, which can easily be recovered by conventional Error correction code (ECC). The proposed 11T cells fully eliminate the HS issue and also prevent the floating node condition of the storage nodes as explained here.

1) Previous power cut-off 11T cell [17]: The previous 11T cell [17] uses the cross-point addressed write access to eliminate write HS disturb. Fig. 3 shows the CHS cell under write '1' operation. The power cut-off switches, MP3 of the CHS cells will also be turned off. If QB stores '0', it would safely maintain it. However, if QB is storing '1', it will become floating and the voltage level will start to degrade. This problem of floating node will be much severe under parameter

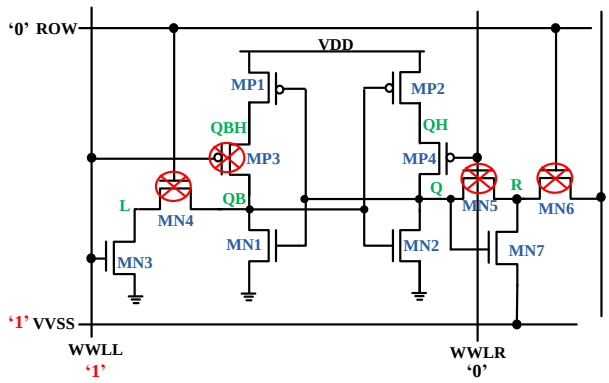

Fig. 3. Column Half-selected cell under write '1' opeartion for previous power cut-off 11T cell [17].

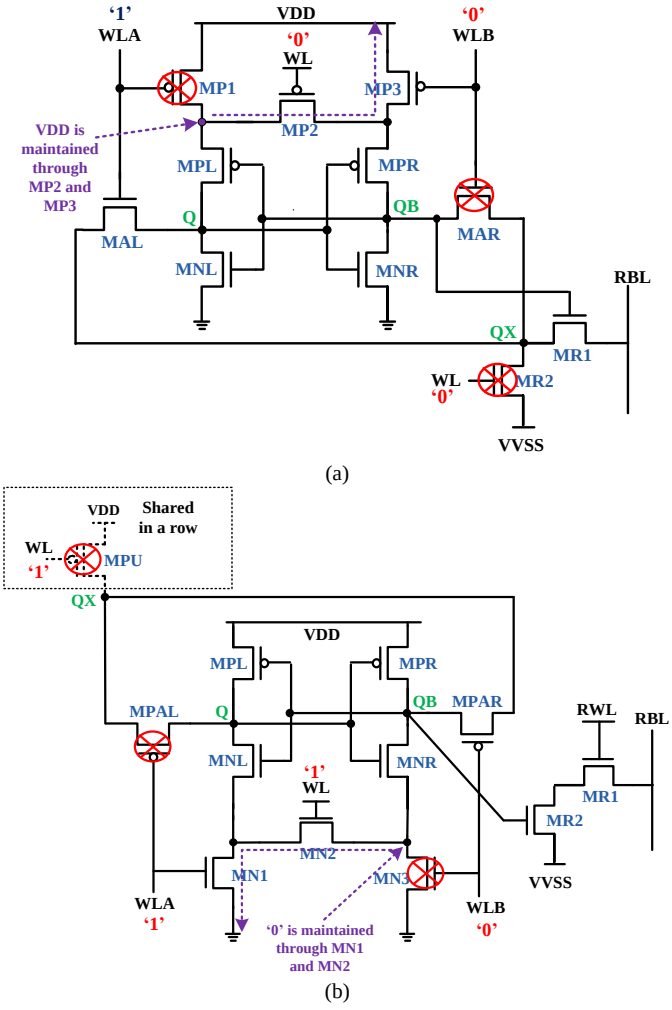

Fig. 4. Column Half-select cell under write '0' operation in (a) 11T-1 (b) 11T-2 cell.

fluctuation at low supply voltages and may lead to flipping of data. Fig. 5 shows the simulated transient waveform of CHS cells of various SRAM cells with 5,000 run of Monte- Carlo simulation at TT, 25°C (simulation is performed for 16nm CMOS predictive technology model [24]). Similarly under write '0' operation, MP4 of CHS cell will be off and node Q

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suffers from floating-'1' situation. However, the voltage level decrease at node Q will be relatively slower because node R is also being pulled up by MN7 due to high voltage level of VVSS. Therefore, in this case, the data retention time, which is the time up to which the nodes can retain data without flipping, will be relatively longer. In Fig. 5, it is shown that, in the CHS cell of 11T cell [17], floating nodes for the case of Q=1 and Q=0, both are not recoverable and lead to flipping of data. Therefore, for this cell, robust operation of CHS cells cannot be achieved at nanoscale technologies.

2) *11T-1 cell*: For RHS cells, the write access transistors in proposed 11T-1 cell are off and cell core is isolated from any disturbing path. Fig. 4(a) shows CHS cell under write '0' operation of 11T-1 cell. The signal WLA is high, whereas WL and WLB are low. The access transistor MR2 is off as WL is '0'. Since MR1 is also off for the case of Q=1, write disturb path does not exist. However, for the case of Q=0, MR1 will be on and Q will be directly accessible to RBL. Still Q will not be disturbed since RBL is also at '0'. Moreover, the PMOS switch MP1 is off, which breaks the pull-up path for left inverter. However, the floating avoidance assist switch, MP2 is on as WL is low, which helps to maintain the pull–up path and avoids floating of Q. Similar operation is observed for write '1' case also due to symmetry of CHS cells in proposed 11T-1. Fig. 5 shows that, floating Q=1 (also QB=1 under write '1' operation) in CHS cell of 11T-1 has been completely recovered and no case of data flip is observed for a run of 5000 MC simulations.

3) *11T-2 cell*: Similarly, for RHS cells in proposed 11T-2 cell, MPAL and MPAR both are off and cell core is free from any disturbing path. Fig. 4(b) shows CHS cell under write '0' operation of 11T-2 cell. Since MPU is on only for the selected rows, CHS cells will be completely isolated from the write disturb path. As shown in Fig. 4(b), WLB is '0', which breaks the pull-down path by turning MN3 off. If QB stores '0', it may float during write access, but floating avoidance switch MN2 helps to maintain the '0' level of the floating node. Similar operation will happen during write '1' operation, where '0' of left inverter is maintained through MN2 and MN3. Fig.5 shows that, floating QB=0 (also Q=0 under write '1' operation) in CHS cell of 11T-2 has been completely recovered and no case of data flip is observed for a run of 5000 MC simulations.

III. BTI ANALYSIS FRAMEWORK

NBTI primarily occurs when negative bias is applied to the gate of PMOS transistor while PBTI occurs in NMOS when gate of transistor is stressed with positive bias. This condition is called stress mode which increases the threshold voltage of the transistor. BTI induced degradation is partially recovered when stress condition is reversed i.e. PMOS is positive biased and NMOS is negative biased. When gate-source voltage of PMOS transistor is negative, holes from the inversion layer breaks Si-H bond at Si-SiO2 interface and lead to the formation of interface traps. These traps are positive in nature and manifests with increase in the threshold voltage of the transistor. In poly gate, PBTI is negligible but with the

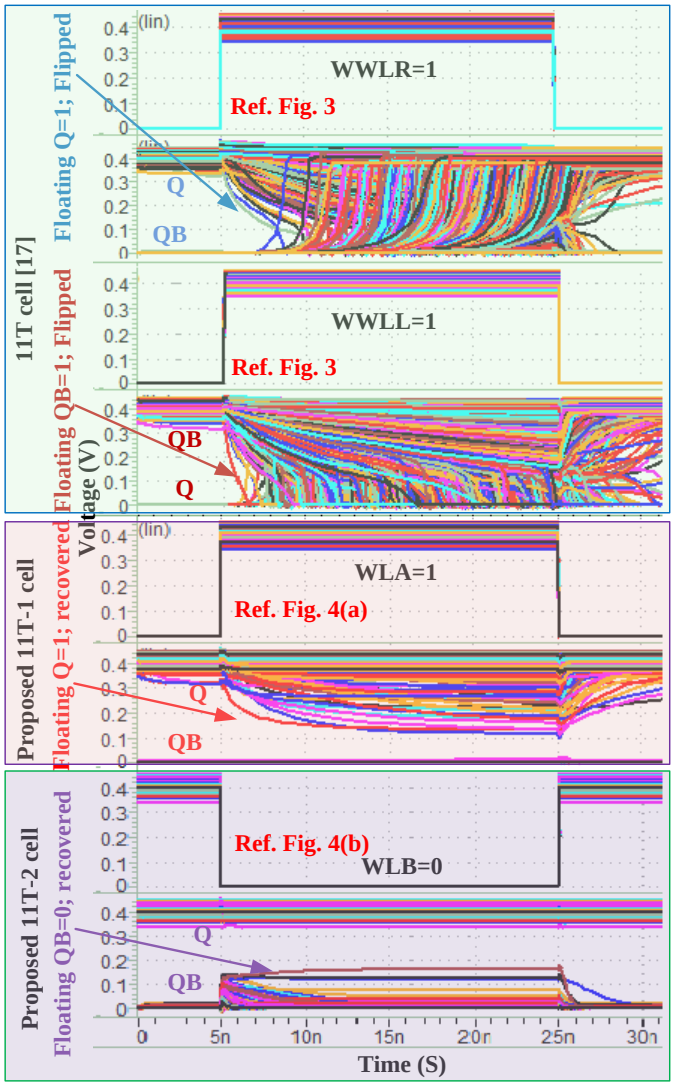

Fig. 5. Simulated transient waveform of Column Half-selected cells of various SRAM cells showing floating node conditions at TT, 25° C, and V_{DD}=0.4V.

introduction of high-*k* metal gate, PBTI has become more than NBTI. Recently, a physics based model consisting of uncorrelated trap generation (TG) and trapping (electron and hole) has successfully explained DC and AC NBTI (PBTI) [25]. This model is in accordance with the reaction diffusion (R-D) model under static and relaxed stress for modelling BTI. It follows same time exponent of n, which is approximately equal to 0.16, as shown in equation (1) [26].

$$\Delta V_{th}(t) \cong K_{ac} \times t^{n} \cong \alpha(S, f) K_{dc} \times t^{n} \qquad (1)$$

Where K_{dc} is technology-dependent constant and 'n' is the time exponent parameter. Activity factor $\alpha(S, f)$ is the AC degradation factor, which is the function of signal duty cycle (S) and frequency (f). However, the effect of frequency on the ΔV_{th} is found to be negligible [25]. Therefore, dependence of activity factor on signal duty cycle can be approximated as given in equation 2 [27].

$$\alpha(S, f) \cong S^{1/6} \qquad (2)$$

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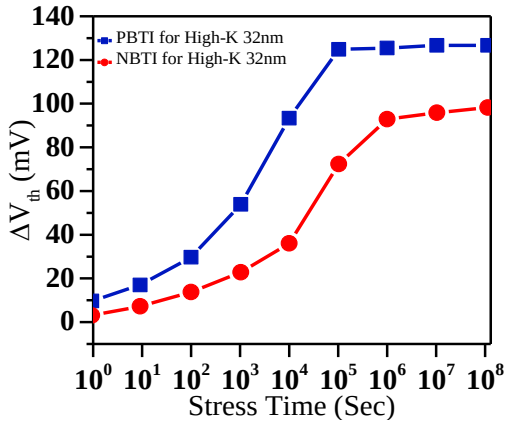

Fig. 6. Threshold voltage shift due to NBTI and PBTI for high-K and poly gate in 32nm technology node [28].

Fig. 6 shows the threshold voltage shift of 32nm high-*k* metal gate transistor under static stress due to BTI, which has been calibrated with published data in [28] and this data is used to analyze the effect of aging in SRAM cell. It is also to be noted that, $\Delta V_{th}(t)$, as given by equation 1 is calibrated with the data of Fig. 6 till the time when it saturates. Once $\Delta V_{th}(t)$ saturates, it is assumed to be constant and independent of time. We have performed the simulation by assuming the saturated value of $\Delta V_{th}(t)$ after this time. This is primarily the reason for saturation in the simulation results as discussed in section IV. Fig.7 shows the simulation flow used in this paper to analyze the effect of BTI based on 32nm PTM high-*k* metal gate model [24]. Depending upon the stress condition, temperature and power supply, we first extracted the shift in the threshold voltage of each transistor, which was then added to the nominal threshold voltage of the model card. The modified model card was then used for the BTI simulation to study the aging effect on various SRAM performance metrics.

In simulation, we have considered various probabilities of data to be stored at Q and QB nodes to extensively analyze the change in SRAM performance metrics due to BTI. There are various probabilities of data to be stored on this node and it is categorized into static and relaxed stress.

1) Static stress: It has been assumed that the cell stores Q='0' and QB='1'for long time interval as shown in Fig. 8. The transistors MNL and MPR are severely degraded due PBTI and NBTI respectively. Since, the read operation doesn't affect the state of data stored on this node; it contributes equally to the static stress. However, this condition is not realistic for SRAMs as only reading and holding of data are not its purpose.

2) Relaxed stress: In this case, it is considered that the cell flips the data constantly and all transistors in cross coupled inverter are under partial stress. Three stress conditions are chosen namely 10/90, 25/75, 50/50. Here, 10/90 signifies that cell stores Q='1' for 10% of the time and Q='0' for 90% of the time, which means that MPL and MNR (Fig. 8) are under stress for 10% of the time and relaxed for the remaining time. Similarly, MPR and MNL are under stress for 90% of the time and relaxed for the remaining time. We have performed the aging simulation mostly under relaxed stress condition. Stress on access transistors is ignored since these are under stress only when word line is high which is negligible compared to

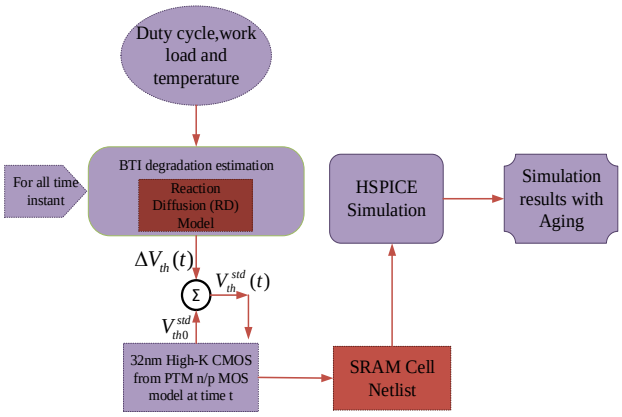

Fig. 7. Simulation flow for BTI analysis.

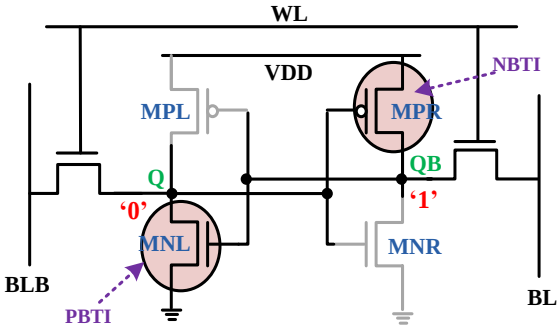

Fig. 8. 6T SRAM cell showing stress on transistors due to NBTI and PBTI.

TABLE II
VARIATION IN PARAMETERS FOR MONTE-CARLO SIMULATION

	Parameters	Nominal value	Relative variation (in percentage)	Type
Local Variations	Channel length (L), Channel width (W) (in nm)	32 W	10	Independent normal Gaussian distribution
	Channel doping – concentration (NDEP) (in cm^{-3})	(4.12e+018, 3.07e+018)*		
	Oxide thickness (T_{OX}) (in nm)	1.15		
	Threshold voltage (V_{th0}) (in Volts)	(0.49396, -0.49155)*		
Global Variations	Supply voltage (V_{DD}) (in Volts)	0.9	10	Independent normal Gaussian distribution

W is according to the size of transistor as discussed in section V
*(for NMOS and PMOS respectively)

SRAM's lifetime [29]. Time duration of 10^8 seconds (approx. 3 years) is considered for all BTI simulations.

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IV. SIMULATION RESULTS AND DISCUSSION

In this section, the impact of BTI on various performance metrics of SRAM cells is considered. Monte-Carlo (MC) simulations with a sample size of 5000 have been performed to analyze the impact of process variations on the performance metric of cells, at t=0s as well as at t= 10^8 s. At t=0s, the V_{th} shift due to aging is zero, therefore, threshold deviation will be only due to time-zero variability. Since, our design is in

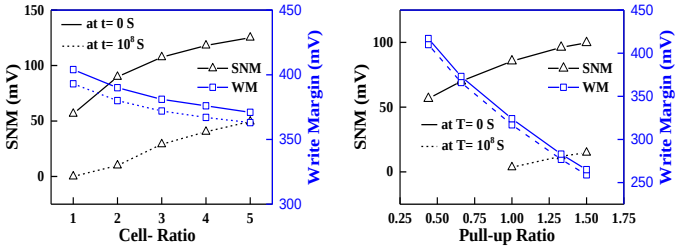

Fig. 9. SNM and WM of 6T SRAM cell as a function of CR and PR.

nanometer regime, to capture correlated effect, we have also taken into account the 3σ variation in other parameters along with V_{th0}, as given in Table II [30], [31]. However, at t= 10^8 s, BTI-induced V_{th} shift is observed as shown in Fig.6. 3σ variation of 10% around the mean value of aging-induced threshold shift, $<\Delta V_{thA}(t)>$ is assumed here, with independent Gaussian distributions. The aging-induced V_{th} variation is modelled as

$$\Delta V_{thA}(t) = N(<\Delta V_{thA}(t)>, \sigma \Delta V_{thA}(t)) \quad (3)$$

All simulations other than MC transient simulation plot (Fig. 5) are performed using 32nm predictive technology model (PTM) [24].

A. Transistor Sizing Analysis

Proper device sizing is a necessary requirement in SRAM cell design for a careful balance of read stability and write-ability. The SRAM cell sizing is defined in terms of cell ratio (CR) and pull-up ratio (PR), which are denoted as CR= $(W/L)_{pull\text{-}down}/(W/L)_{access}$ and PR=$(W/L)_{pull\text{-}up}/(W/L)_{access}$. Generally, to achieve good read stability, large CR is preferred to reduce read disturbance. On the other hand, to achieve good write-ability, a strong access-transistor and relatively weaker pull-up transistor (low PR) are desired. Typically, CR of 1.2–3 is required to avoid read-disturb [32] and PR ≤ 1.8 is required to maintain good write-ability [33]. Fig. 9 plots the static noise margin (SNM) and Write-margin (WM) of 6T SRAM cell for varying CR and PR. It is observed that SNM improves significantly but WM decreases with increasing CR. We can find an optimum value of CR and PR from this plot to achieve a good balance between SNM and WM. It is also worthy to mention that the optimum value of CR and PR for obtaining best SNM and WM increases due to BTI. For maintaining appreciable read stability and write-ability, CR = 1.33 and PR = 0.67 are taken for 6T SRAM cell, as adopted by authors in [31], [34].

However, the proposed cells use separate read buffers for the read operation, therefore, read disturb problem is of no concern. The cell operation is not limited by read-write

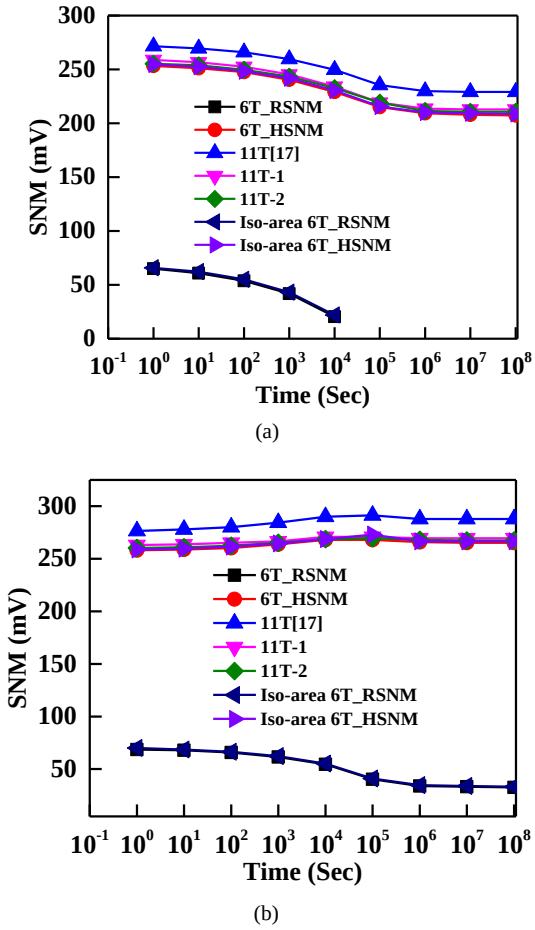

Fig. 10. SNM as a function of stress time under condition of (a) static stress (b) relaxed stress of 10/90.

conflict sizing requirement and sizing can be done depending on desired write-performance and area constraint. Minimum sized devices for the cell core are used to minimize the area and leakage overhead. To reduce access delays, the access transistors are upsized but it leads to increase in bitline capacitances. Therefore, only 1.5× upsized access transistors are used to balance between access delays and bitline-capacitances. In 11T-1 cell, MP1, MP2 and MP3 are power cut-off switches to just break the pull- up path during write operation and to supply enough pull-up current to maintain the data in column half-selected cells. Therefore, minimum size devices for these transistors are used. For the same reason, minimum width is used for MN1, MN2 and MN3 in 11T-2. The transistor MPU in 11T-2 cell is of wider width, so that it can provide high pull-up current to the cell node during write-access.

In the subsequent sections, we have also performed Iso-area analyses and compared the performance of proposed cells with Iso-area 6T cell (upsized bitcell to have same area as 11T-1 cell). Since 6T suffers with conflicting read and write requirements as observed from Fig. 9, all transistors in the 6T minimum sized cell are upsized by the same factor to improve the read-stability and write-ability simultaneously.

B. Static Noise Margin

Static noise margin (SNM) is the minimum dc noise voltage that can flip the data in an SRAM cell. For robust operation,

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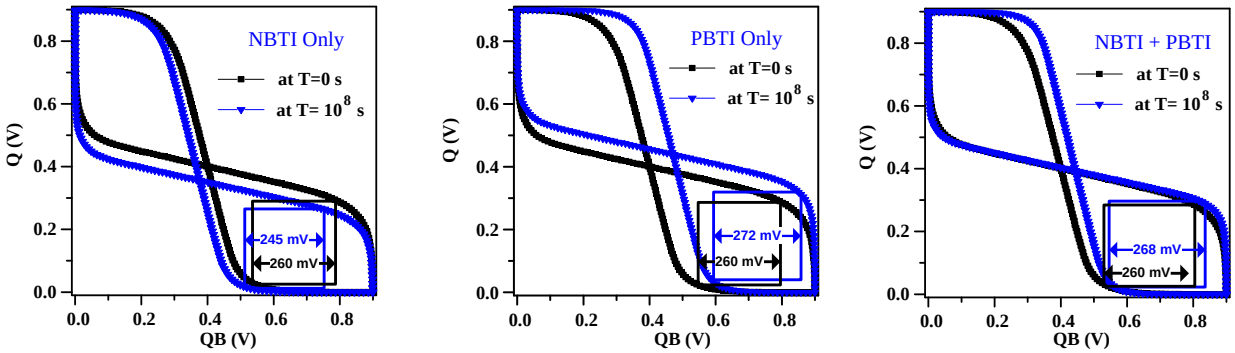

Fig. 11. Shifts in Butterfly curve to measure HSNM of 6T (RSNM/HSNM of 11T-1 or 11T-2) over the stress period of 3 years.

TABLE III
COMPARISON OF PERCENTAGE CHANGE IN SRAM PERFORMANCE METRICS DUE TO AGING OVER THE STRESS PERIOD OF 3 YEARS

SRAM Cells	Read SNM			Write margin			Write access Time			Read Access Time		
	Stress Condition on Inverter-Pair Transistors											
	10/90	25/75	50/50	10/90	25/75	50/50	10/90	25/75	50/50	10/90	25/75	50/50
6T	-53.5 (3.5)	-39.8 (7.7)	-25.2 (11.8)	14.2	16.6	18.8	16.0	15.9	13.9	17.7	16.7	15.0
Iso-area 6T	-53.4 (3.5)	-40.6 (7.7)	-25.7 (11.8)	11.5	13.8	16.0	10.2	9.4	8.3	30.4	29.7	30.4
11T[17]	4.9	8.5	12.6	8.5	9.0	9.3	50.3	47.0	45.7	-0.01	-0.01	-0.01
11T-1	2.7	7.3	11.4	7.2	7.3	7.5	38.1	37.3	35.6	-0.02	-0.04	-0.04
11T-2	3.3	7.4	11.5	13.2	13.4	13.7	23.3	26.6	29.7	0.0	0.0	0.0

'-ve' signifies the degradation (.) is HSNM

SRAM cell should have high SNM. SNM is categorized as Hold SNM (HSNM) and Read SNM (RSNM), which are calculated during Hold and Read operation respectively. Since the 11T cells discussed in this work are read decoupled, their RSNM and HSNM are equal. However, for 6T cell, these values are quite different. Fig. 10 shows the change in SNM of SRAM cells over the stress time due to BTI. First, we consider static stress so that only MNL and MPR suffer continuous stress. The trip point of the right inverter will reduce due to increased V_{th} of MPR, whereas that of left inverter will be raised due to increased V_{th} of MNL. The butterfly curve will be asymmetric with one lobe significantly smaller. Hence, RSNM (or HSNM) of all the SRAM cell will be degraded due to BTI as shown in Fig. 10(a). A similar degradation of approximately 18.8% is observed in the HSNM of 6T, 11T-1 and 11T-2 cells due to their similar core for storing data. However, 11T [17] cell achieves relatively larger RSNM (HSNM) and attains degradation of 16.4%. This is attributed to its improved inverter characteristic due to PMOS stacking in pull-up path of inverter. The RSNM of 6T cell is considerably low and shows a degradation of 71% owing to high chances of read failure. This is primarily because, 6T is not read decoupled, where read-operation involves significantly increased voltage noise at Q due to increased V_{th} of pull-down transistor MNL. For Iso-area 6T cell, no improvement in RSNM (or HSNM) is observed as the CR remains the same. It is also important to mention that, significant degradation is observed only up to 10^5 seconds, after that degradation is almost negligible. This is attributed to the saturation of V_{th} shift in the model. Now, we consider the condition of relaxed stress of 10/90, where all the transistors of the inverter pair suffer partial stress. The observation is entirely different and it is very interesting to note that, SNM is not being degraded rather improved slightly, when NBTI and PBTI both are considered, as shown in Fig. 10(b). It is also evident that PBTI benefits SNM under relaxed stress. When we consider only NBTI under relaxed stress, MPL and MPR both will suffer degradation. The pull-up path in both the inverters becomes weaker, which reduces the trip points, and the SNM is degraded as shown in Fig. 11(a). Now we consider only PBTI under the same condition. The pull-down transistors MNL and MNR will be degraded and their V_{th} will increase, which causes the trip point to increase for both the inverters. The resulting butterfly lobe will be larger and improved SNM is observed as shown in Fig. 11(b). When NBTI and PBTI both are considered to occur simultaneously, all the transistors of the inverter pair will be degraded. The NBTI occurring in the PMOS of the inverter will tend to reduce the trip point, whereas PBTI occurring in the NMOS of the inverter will tend to increase the trip point. PBTI wins the fight since it causes higher *Vth* shift compared to NBTI (as depicted in Fig. 6) and trip point is increased slightly for both inverters. However, it is clear that, the increase in trip point is not same for both the inverters due to reverse stress. Therefore, the SNM is slightly increased as shown in Fig. 11(c). Table III shows the percentage change in RSNM, WM and Read/Write access time of SRAM cells due to aging (NBTI and PBTI both) under relaxed stress. It can be observed that, as we move from 10/90 to 50/50, the increase in RSNM of 11T [17], 11T-1 and 11T-2 cells is higher due to more relaxation in stress. However, RSNM of 6T cell degrades by more than 60% at 50/50 and for higher stress (as we move towards almost static stress), the degradation approaches to no lobe formation of butterfly curve, and hence, zero RSNM. We also performed the MC simulation to study the impact of process variations on the RSNM of SRAM cells.

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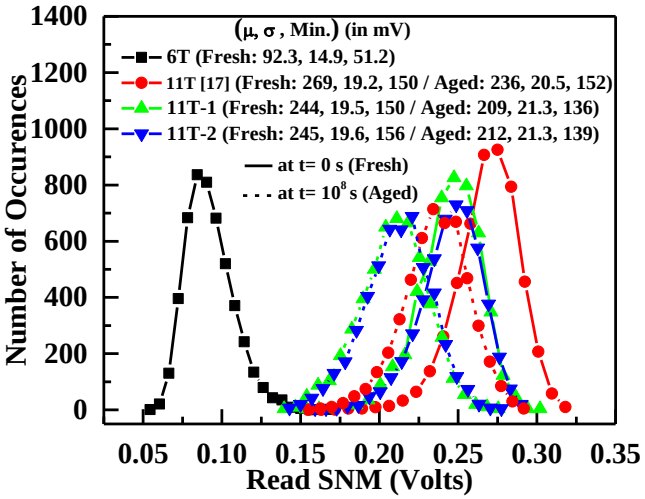

Fig. 12. Statistical distribution plot of RSNM for fresh and aged cell (under worst case static stress) at T=125°C and V_{DD} = 0.9V. (6T suffers read failure due to high degradation at t=10^8 s)

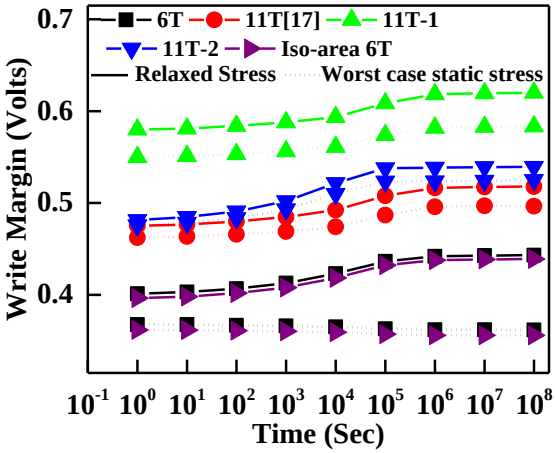

Fig. 13. Write Margin as a function of stress time under the condition of relaxed stress of 10/90.

Fig. 12 shows the statistical distribution of RSNM at 125°C and V_{DD}=0.9V for the fresh as well aged cells. The 6T cell shows worst RSNM due to its conflicting sizing requirement. It is observed that, the 11T [17] shows higher mean RSNM compared with proposed cells 11T-1 and 11T-2. However, the standard deviation and the minimum of RSNM are found to be approximately same for these cells. The read-yield is defined in terms of cell sigma which is the minimum amount of variation that can cause a read failure [35]. For a metric following Gaussian distribution, cell sigma is given by mean (μ)/sigma (σ) [35]-[37]. The 11T [17] cell exhibits highest read-yield among considered cells due to its improved inverter characteristics. The 11T-1 and 11T-2 cells show 2× higher read-yield as compared to 6T cell at V_{DD}=0.9V. We also observe that the mean of RSNM of all the cells degrades by an approximately same factor due to BTI, whereas the standard deviation is slightly increased.

A. Write Margin

Write Margin (WM) is a measure of Write-ability of an

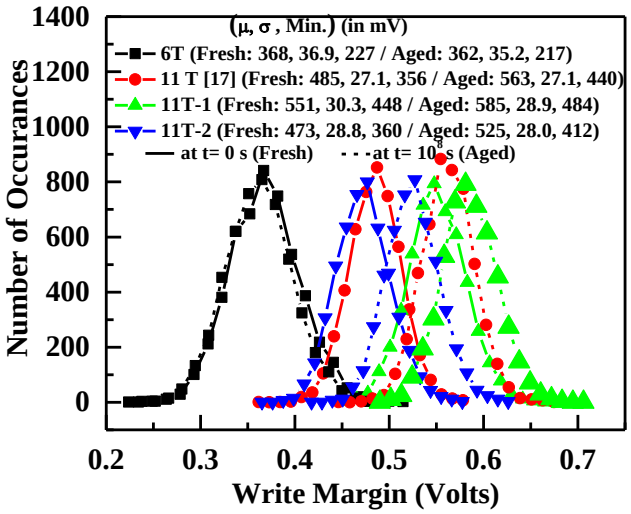

Fig. 14. Statistical distribution plot of WM for fresh and aged cell (under worst case static stress) at T=25°C and V_{DD} = 0.9V.

SRAM cell. To measure WM, data is applied on the bitlines and then wordline (WL) is swept from 0V to V_{DD} (V_{DD} to 0V for 11T-2 cell) that replicates a real write operation. The WM is the difference between V_{DD} and WL voltage (WL voltage in case of 11T-2 cell) at which the nodes Q and QB flip [38]. We first consider the relaxed stress, where both the Pull-up transistors MPL and MPR are degraded. The writing '0' to the node storing '1' becomes easier as pull-up path gets weaker. Hence, WM of the cell increases with time. Fig. 13 shows the increase in WM of SRAM cells over the stress time due to BTI. Now we consider the worst case write scenario, where cell stores Q=0 and QB=1 for a long time so that MPR and MNL age. The cell undergoes write '1' operation immediately followed by write '0' again to get the original value. The second write (write '0') is the worst case write operation as it involves discharging of node Q, for which pull-down path is weaker along with charging of node QB, for which pull-up path is weaker. Therefore, the WM for 6T SRAM cell reduces during the second write for worst case, as depicted in Fig. 13. It is observed that 6T shows a degradation of 2% in the WM over the period of 3 years. The 11T [17] and proposed 11T cells use power cut-off switches for contention-free charging/discharging during write operation and hence their WM is not degraded even for worst case scenario. However, the improvement is now relatively smaller; 7.6%, 6.2% and 11.1% in comparison to the improvement for relaxed stress condition (10/90) which are 9.4%, 7.2% and 13.2% for 11T [17], 11T-1 and 11T-2 cell respectively. In 11T [17], WWLR (data) and ROW signal both are simultaneously pulsed to avoid prior discharge of Q. Whereas in case of 11T-1 cell, the column based WLA/WLB (data) are activated before the WL signal. This causes further ease in the discharge of Q/QB, hence, 11T-1 cell further improves WM in comparison with existing 11T[17]. The 11T-2 cell involves PMOS write access, which is much weaker than its NMOS counterpart at lower supply voltages. Hence, 11T-2 cell shows slightly lower WM than 11T [17]. The Iso-area 6T cell has the same PR as that of its minimum sized 6T cell. Fig. 14 shows the statistical distribution plot of WM based on MC simulation at 25°C and

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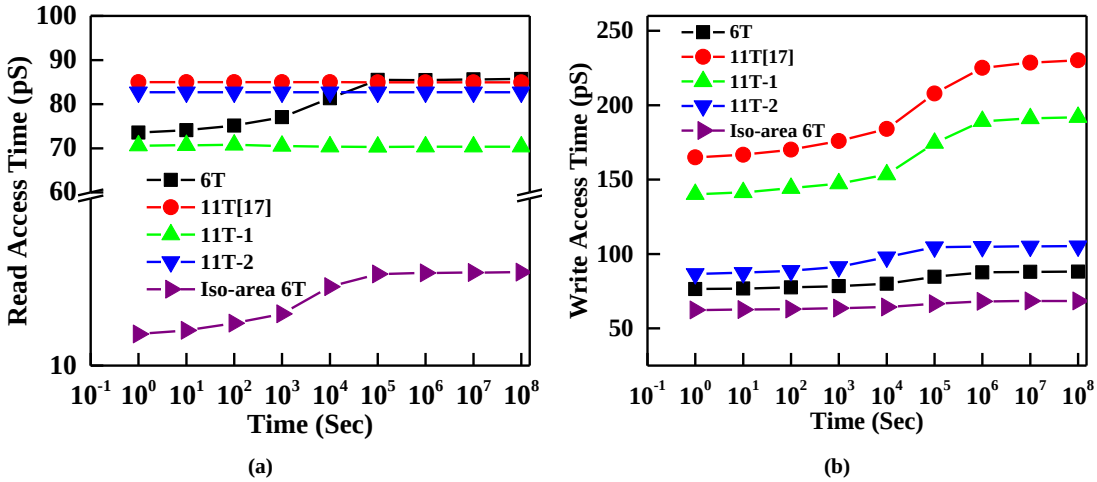

Fig. 15. (a) Read access time (b) Write access time as a function of stress time under condition of relaxed stress of 10/90.

TABLE IV
COMPARISON OF PERCENTAGE CHANGE IN SRAM PERFORMANCE METRICS DUE TO AGING OVER THE STRESS PERIOD OF 3 YEARS

	Write Power			Read Power			Leakage Power		
	Stress Condition on Inverter-Pair Transistors								
SRAM Cells	10/90	25/75	50/50	10/90	25/75	50/50	10/90	25/75	50/50
6T	-29.3	-31.4	-33.0	-14.9	-14.3	-13.2	-51.5	-54.1	-55.9
Iso-area 6T	-28.6	-31.5	-33.7	0.29	0.36	2.0	-51.2	-53.8	-55.6
11T[17]	-33.6	-33.3	-32.6	0.0	0.0	0.0	-72.9	-76.6	-78.9
11T-1	-28.0	-27.7	-27.0	-0.003	-0.003	-0.003	-85.7	-85.1	-83.8
11T-2	-20.4	-22.3	-23.9	0.0	0.0	0.0	-86.9	-87.7	-87.8

V_{DD}=0.9V. The 11T-1 cell shows 49.7% and 13.6% improvement in mean of WM over 6T and 11T [17] cell. The mean (μ) and standard deviation (σ) are extracted from MC simulation to calculate the write-yield as μ/σ of the cells [35]-[37]. The 11T-1 cell achieves 84% and 3% higher write-yield compared to 6T and 11T [17] respectively. The minimum value of WM, for the run of 5000 MC samples, is also highest for 11T-1 cell. Hence, 11T-1 cell is highly robust during write operation in face of process variation.

B. Read/Write Access Time

The read access time or read delay is determined by the time taken by the cell to develop a voltage drop of minimum required voltage (50mV) on the read bitline [20]. The read path in 6T cell consists of access and pull-down transistors. We have discussed that, the node that stores '0' for a long time will have weaker pull-down path due to PBTI of pull-down transistor. This will slow-down the discharging of BL and therefore 6T cell will have increased read delay. On the other side, the 11T [17] and proposed 11T cells use separate read buffer during read access. The read buffer consists of two transistors, MR1 and MR2. MR1 is controlled by row based wordline signal for which the ON duration is very small, therefore its aging is considered to be negligible. Another transistor MR2 is controlled by QB. However, MR2 is also free from aging irrespective of the data stored at QB, because it is in series with MR1, which is stress-free [29]. Hence, BTI has negligible impact on read delay of these cells, which is clearly depicted in Fig. 15 (a). It is also to be noted that, 11T-1 cell shows smallest read delay compared with other considered cells. During the read operation, if QB stores '1', the node QX in 11T-2 cell gets charged before the activation of WL signal. Upon activation of WL, QX is quickly discharged and drop on RBL becomes fast. Therefore, smaller delay is observed in this case as compared to the buffer which has WL driven transistor connected to RBL. We also observe that, the Iso-area 6T cell shows the smallest read delay due to stronger access transistors. However, the BTI induced read delay degradation is very high e.g. 30% for the case of 10/90. Write access time or write delay is estimated as the time duration between the WL activation time to the time when the opposite node (QB) charges up to 90% of V_{DD} or discharges to 10% of V_{DD} depending on data written at Q and whichever is the worse. Fig.15 (b) depicts the change in write access time of SRAM cells due to BTI over the stress time. Considering the case of 10/90, MNL and MPR degrade severely and it takes longer time to charge node QB. Therefore, write delay increases due to BTI. However, the increase in write delay is smaller as compared to read delay for 6T cell, since BTI causes the threshold voltage of PMOS transistors to increase by smaller amount than that of NMOS transistors [28]. The power cut-off 11T [17] and proposed 11T cells show higher increase in write delay as compared to 6T cell due to BTI as shown in Table III. This is because the pull-up path (pull-down path in case of 11T-2) is much weaker due to aging of both stacked transistors. Power cutoff switches are considered to be in stress for 100% of the time as they are off only for the duration of write access and for rest

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TABLE V
COMPARISON BETWEEN THE PROPOSED AND PREVIOUS SRAM CELLS

	6T		11T [17]		11T-1		11T-2	
# Bitlines/Wordlines	3 (2-BL, 1-WL)		5 (3-WL, 1-BL, 1-VVSS)		5 (3-WL, 1-RBL, 1-VVSS)		6 (3-WL,1-RWL, 1-RBL, 1-VVSS)	
WHS free	No		No*		Yes		Yes	
Normalized cell area	1		2.32		2.43		2.28	
	Fresh	**Aged**	**Fresh**	**Aged**	**Fresh**	**Aged**	**Fresh**	**Aged**
Read yield#	6.19 σ	$	14.01 σ	11.5 σ	12.5 σ	9.8 σ	12.5 σ	9.95 σ
Write yield#	9.9 σ	10.2 σ	17.8 σ	20.7 σ	18.2 σ	20.9 σ	16.9 σ	18.8 σ
Read access time (in ps)	72.8	85.7	85.0	84.9	70.5	70.3	82.7	82.7
Write access time (in ps)	75.9	88.1	162	230	139	192	85.4	105
Leakage Power (in nW)	36.9	17.9	10.8	2.9	12.8	1.84	12.3	1.61

*Not fully write- half-select (WHS) as floating-1 condition is encountered in column write-half-selected cells
#Read/write yield is evaluated in terms of cell sigma (μ/ σ) as suggested in [36], [37].
$6T suffers high read failure due to high degradation at t=10^8 s. **Fresh**: at t=0s, **Aged**: at t=10^8 s

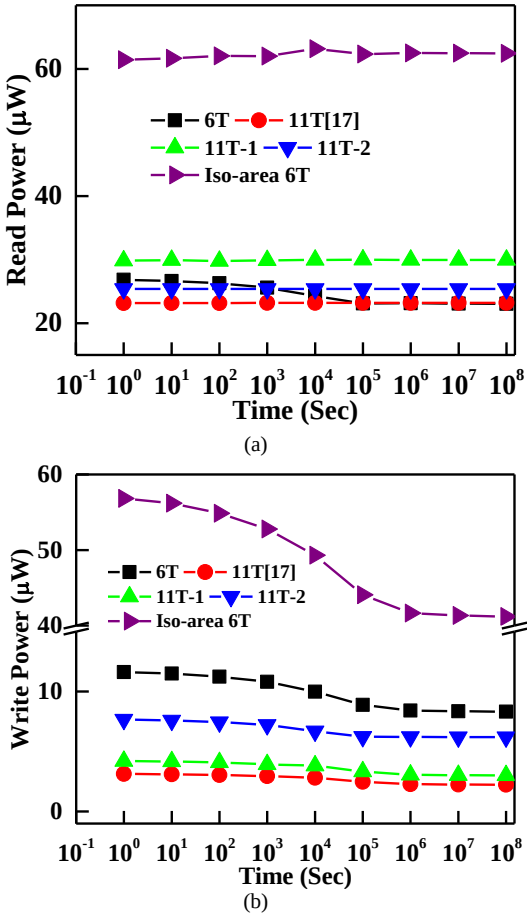

Fig. 16. (a) Read power (b) Write power as a function of stress time under condition of relaxed stress of 10/90.

of the time they are on. It is also worthy to observe that, as we move from 10/90 to more relaxed stress condition 50/50, the delay is reduced due to the smaller degradation of pull-up transistors (pull-down transistors in 11T-2 cell).

E. Read/Write power

Fig. 16 depicts the change in read/write power consumption of the cells. We have discussed that, the transistors forming the read path are stress-free in 11T [17] and proposed 11T cells. BTI has almost no effect on the read power of these cells.

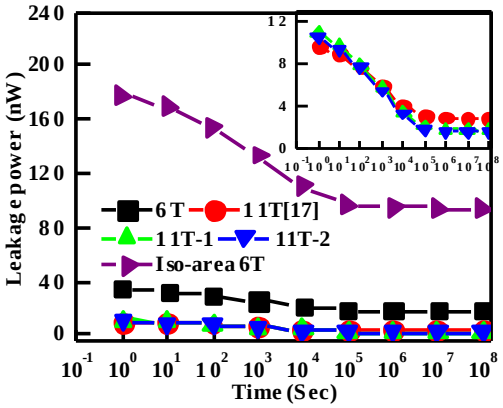

Fig. 17. Leakage power as a function of stress time under condition of relaxed stress of 10/90. (Inset: Expanded y-axis to clearly see the data)

However write power considerably reduces over time due to BTI induced V_{th} increase of the transistors. Since, there is always a trade-off between power and delay, read/write power for 11T [17] cell is found to be smaller than the proposed cells. However, 11T-1 (11T-2) consumes 64% (34%) smaller write power as compared to 6T cell.

F. Leakage power

Leakage power contributes largely to the total power dissipation in an SRAM cell because a major part of the cache remains in standby mode for most of the time [31]. Hence, it is also very important to see the BTI impact on leakage power. Considering the situation of static stress, where the state of the cell is fixed and two of the inverter pair transistors are permanently ON. It is observed that, BTI has a negligible impact on leakage power as V_{th} increase due to BTI only happens in ON transistors, which contributes very small to the leakage. However, for the relaxed stress condition, BTI induced V_{th} increase happens in all the transistors of the inverter pair, and therefore, reduction in leakage is observed as shown in Fig. 17. In 11T-1 and 11T-2 cells, VVSS and RBL both are high during the hold mode, which shuts the leakage in the access path. The leakage contribution of cross coupled inverter is reduced due to the PMOS stacking in the pull-up path and NMOS stacking in the pull-down path respectively in 11T-1 and 11T-2 cells. It can be observed from Table IV that, the proposed cells achieve larger reduction in leakage due to

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BTI, a figure of 85.7% and 86.9% in comparison to 75.9% reduction in 11T [17] cell for 10/90 stress condition.

G. Cell Area comparison

Fig.18 shows the layout view of 6T, 11T [17] and the proposed 11T cells designed using 45nm technology rules. Each redrawn Min-cell area is normalized to 6T. Table V compares the normalized cell area along with other important performance metrics of various SRAM cells. In order to route the row based signals, one higher metal layer is used in the layout of 11T [17] and proposed 11T cells. The proposed cells 11T-1 and 11T-2 show an area overhead of 2.58× and 2.42× as compared to 6T SRAM cell. The 11T-1 cell exhibits 4.8% higher area as compared to 11T [17] cell. However, it has other useful features such as floating avoidance necessary for the stability of HS cells, high WM and lower access delays. The 11T-2 cell occupies 2% smaller area as compared to 11T [17] cell. However, in the cell area, we have ignored the area consumed by the row shared access transistor MPU. To include this area, PMOS transistor is drawn within the row pitch at the extreme left of a row. This transistor is made four times larger than the minimum size pull-down NMOS to enhance its strength so that it can supply sufficient current to charge the storage node. In this case, an additional 1.3% area overhead per cell is found, if this transistor is shared among 16 cells in a row.

V. CONCLUSION

This work proposed two fully half-select-free robust 11T SRAM cell topologies that are suitable for bit-interleaved architecture. The proposed 11T-1 and 11T-2 cells eliminate Read disturb, Write half-select disturb and improves the Write-ability by using power-cutoff and write '0'/ '1' only techniques. The 11T-1 and 11T-2 cells have shown higher read and write yields compared with 6T cell. Both the proposed cells successfully eliminate the floating node condition encountered in earlier power cut-off cells during write half-select. Monte-Carlo simulation confirms low-voltage operation without any additional peripheral Write-and Read-assist circuits. The impact of BTI on the SRAM performance was also analyzed in a predictive 32nm High-*k* metal gate CMOS technology. Under static stress, the RSNM is found to be reduced for all cells. However, interestingly it was found that 11T-1 and 11T-2 cells have improved RSNM due to BTI. Moreover, the proposed cells improve WM, reduce write power and leakage power, increases write delay without any effect on read delay/power over time. The MC and BTI analysis have demonstrated that the proposed 11T cells could be an excellent choice for reliable SRAM design at nanoscale technologies amidst process variations and transistor aging effect.

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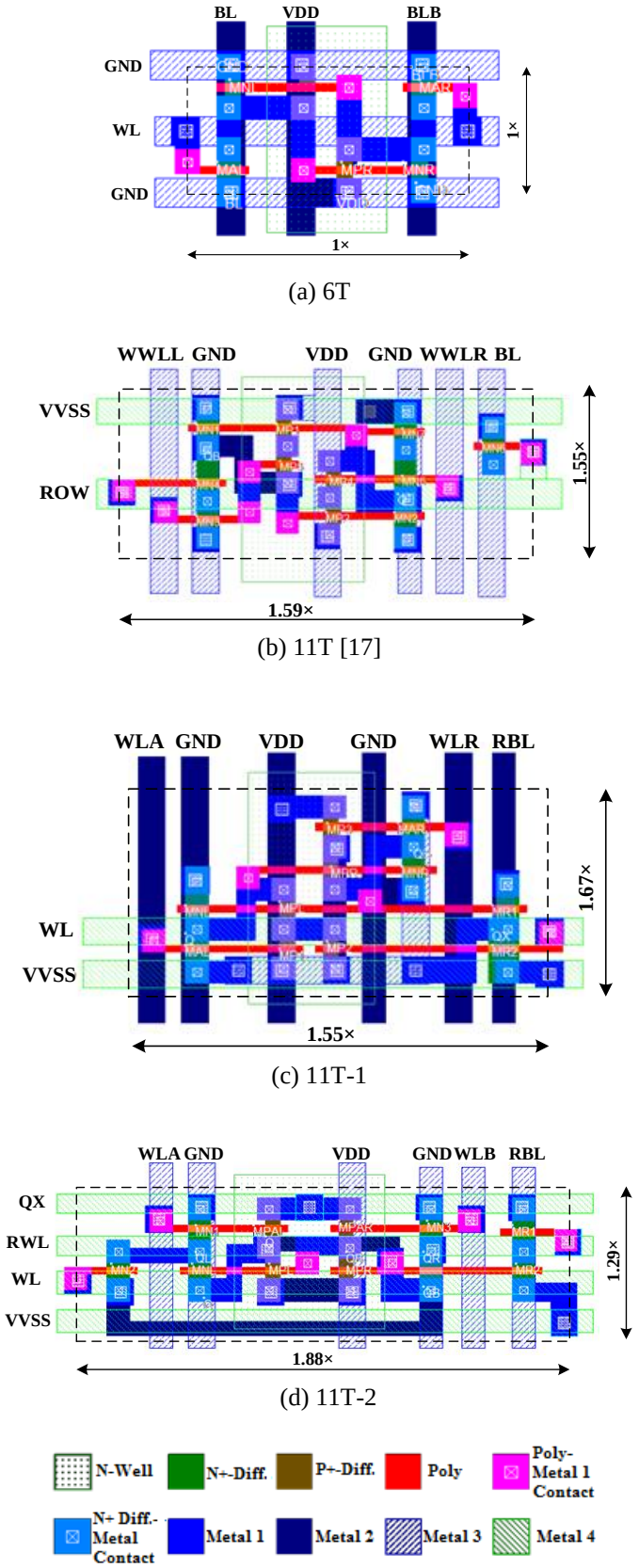

Fig. 18. Layout of (a) 6T, (b) 11T [17] (c)11T-1 (d) 11T-2 SRAM cells.

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