Novel Radiation-Hardened-by-Design (RHBD) 12T Memory Cell for Aerospace Applications in Nanoscale CMOS Technology

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Abstract—In this paper, a novel radiation-hardened-by-design (RHBD) 12T memory cell is proposed to tolerate single node upset and multiple-node upset based on upset physical mechanism behind soft errors together with reasonable layout-topology. The verification results obtained confirm that the proposed 12T cell can provide a good radiation robustness. Compared with 13T cell, the increased area, power, read/write access time overheads of the proposed 12T cell are $-18.9\%$, $-23.8\%$, and $171.6\%/-50.0\%$, respectively. Moreover, its hold static noise margin is 986.2 mV which is higher than that of 13T cell. This means that the proposed 12T cell also has higher stability when it provides fault tolerance capability.

Index Terms—Memory, multiple-node upset, radiation-hardened-by-design (RHBD), soft errors.

I. INTRODUCTION

MEMORIES are extensively used in aerospace applications as the medium to store data in which single event upsets (SEUs) induced by radiation particles are becoming one of the most significant issues [1]–[5]. Because they can conduce to the data corruption in a memory chip and the circuit itself is not permanently damaged, SEUs are also described as the soft errors [1]. Therefore, SEUs can cause a malfunctioning of an electronic system. In some critical memory applications (e.g., satellite equipment [5], [6] and cardioverter defibrillators [7]), SEUs can be detrimental and crucial.

However, radiation hardening techniques for memories are one of the bottlenecks in providing fault tolerance.

For many years, some radiation-hardening-by-design (RHBD) techniques have been used to tolerate soft errors in memories using standard commercial CMOS foundry processes, with no modifications to the existing process or violation of design rules [6]. Traditionally, these techniques can be mainly divided into the following three subitem techniques.

1) Layout-level techniques employ mainly layout changes, such as H-gate, T-gate, annular-gate, and shallow trench isolation (STI) for the radiation tolerance [8], [9]. Although it is generally true that these layout-level techniques do provide partial protection capability, they are difficult to implement in nanometer technologies due to more exigent design rules.

2) The first circuit-level technique is triple modular redundancy (TMR) which is used for mitigating SEU in memories or latches [10]. This hardening technique relies on three copies of memory cell to store the same data, and a voting circuitry to determine the right output. If one cell is upset, the remaining two copies still remain unchanged from the initial data. Then, the voting is executed by the majority voting process so that the stored data can be output rightly. The main issue of TMR is that it has to incur a large area overhead and power dissipation [11]. The most common circuit-level hardening techniques are to add extra redundant transistors based on standard 6T cell or to propose new hardened memory cells. For example, Jahinnuzaman et al. [12], have proposed a 10T hardened memory cell using ten transistors. However, it can only recover $1 \rightarrow 0$ SEU. In [13], PS-10T and NS-10T hardened memory cells are proposed to provide only partial SEU robustness. In others words, PS-10T cell can only recover $1 \rightarrow 0$ SEU and NS-10T cell is only capable of recovering $0 \rightarrow 1$ SEU. In [14], the dual interlocked storage cell (DICE) is proposed, which utilizes 12 transistors to obtain fault robustness in any one single node. Recently, 11T and 13T cells are, respectively, proposed in [15] and [16] using single-ended memory structure. Compared with 11T cell, the sharing critical charge of 13T cell is slightly increased due to the hysteresis effect of the Schmitt trigger. Rajaei et al. [17] have optimized
the structure of 13T memory cell to propose a new hardened memory cell (R13T). Compared with 13T cell, R13T cell has more shared critical charge. However, the main drawback of these cells is that they cannot tolerate a multiple-node upset. In [9], by using circuit-level hardening technique together with layout-level STI approach, an RH12T memory cell is proposed to tolerate a multiple-node upset. However, this memory cell has more area overhead and lower stability.

3) System-level techniques mean that they utilize some error detection and correction codes (ECCs) to tolerate soft errors at the system-level architecture [18]–[20]. However, ECC techniques would require more overheads especially for time performance (nanosecond-level delay), since the encoding and decoding circuits are more complex [21]–[24]. This means that the time performance of memory will be affected severely.

In general, compared with layout- and system-level hardening techniques, the advantage of circuit-level RHBD memory design is that it can provide not only higher fault tolerate capability, but also lower overheads especially for time performance (picosecond-level delay). Therefore, in this paper, we focus on proposing a novel circuit-level RHBD 12T cell to improve the SEU robustness of memories.

The remainder of this paper is mainly divided into the following sections. Section II introduces the proposed RHBD 12T cell structure, write/read timing, and SEU recovery analysis. In Section III, the SEU recovery simulations, and the detailed performance comparisons for various memory cells are shown. Finally, some conclusions are presented in Section IV.

II. RHBD 12T MEMORY CELL DESIGN

A. Cell Schematic and Write/Read Timing

The proposed RHBD 12T memory cell is shown in Fig. 1. Here, two access transistors, pMOS transistors P5 and P6, have been connected bit-lines BLN and BL to the output nodes QN and Q, respectively. Their on/off state is determined by a word-line WL. It should be noted that when a radiation particle strikes pMOS transistor, only a positive transient pulse (0→1 or 1→1 transient pulse) can be generated; on the contrary, only a negative transient pulse (1→0 or 0→0 transient pulse) can be induced when a radiation particle strikes nMOS transistor [2]. Therefore, in order to avoid a negative transient pulse induced by a radiation particle in Q and QN nodes, pMOS transistors (i.e., transistors P6 and P5) are used as access transistors.

Considering the stored 1 state (i.e., QN = 0, Q = 1, S0 = 0, and S1 = 1) for the proposed RHBD 12T cell (see Fig. 1).

1) When word-line WL is high state 1, transistors P1, P4, P7, N2, and N3 are ON, and the remaining transistors are OFF. Thus, nodes Q and QN are not changed, and they also stored their original data, respectively.

2) Before read operation is executed in the proposed 12T memory cell, two bit-lines BL and BLN need to be precharged to supply voltage VDD. After read operation, and word-line WL is 0 state, the output node Q will store its original state 1 without changing. However, because transistors P5, P7, and N2 are ON, bitline BLN will be discharged. Next, when the voltage difference between two bit-lines BL and BLN are obtained, the differential sense amplifier in memories will output the stored data.

3) To write data 0 into the proposed 12T cell, word-line WL and bitline BL need to be 0 state, and bitline BLN must be 1 state. Subsequently, node Q will be pulled down to 0 state, and node QN will be pulled up to 1 state. Transistors P2, P3, P8, N1, and N4 will be ON, and transistors P1, P4, P7, N2, and N3 will be OFF. When word-line WL is pulled back to high state 1, the stored data will be 0. This means that data 0 can be successfully written into the proposed RHBD 12T memory cell.

Fig. 2 shows a “write 0, read 0, write 1, and read 1” transient simulation result. From Fig. 2, we can see that the proposed cell can rightly achieve write and read operations.

B. SEU Recovery Analysis

In this section, the SEU recovery analysis results for the proposed RHBD 12T memory cell are presented. Considering the state shown in Fig. 1, node Q is not a sensitive node, because it is connected with the drain area of OFF pMOS transistors P6 and P8, and its stored value is 1 state. Therefore, according to the upset physical mechanism, when node Q is strike, only a positive pulse is induced, i.e., node Q will be affected by a 1→1 transient pulse so that the stored value of node Q is not changed.
1) When node QN is upset by a radiation particle, node QN will be pulled up to state 1, then transistors P1 and P4 will be OFF. Subsequently, nodes Q and S1 will remain the original logic 1 state without losing voltage value. Therefore, transistor N3 will not be OFF, and node S0 keeps its original 0 state. Transistor P7 and N2 will be ON state, and then, node QN will be pulled back to its original state 0.

2) When a radiation particle strikes node S0, its value will be changed. Then, transistor P7 is temporarily turned OFF, and transistor N1 is temporarily turned ON, and thus, node S1 will be pulled down to 0. However, because of capacitive effect, node QN will not be changed to 1 state, and transistors N4 and P1 keep their OFF and ON states, respectively. Therefore, node Q will be unchanged through ON transistor P4, and node S1 can recover to initial 1 state. Finally, transistor N3 are turned ON, and node S0 will be pulled back to its original 0 state.

3) When the state of node S1 is changed to 0 from original 1 state by a radiation particle, transistors N3 and P8 will be turned OFF and ON, respectively. Because the voltages of nodes Q, QN, and S0 will be unchanged, transistor P1 remains ON. Therefore, node S1 will be pulled back to its original 1 state through ON transistor P1.

4) When a radiation particle strikes a semiconductor device because of charge sharing effect, multiple sensitive nodes may be affected. In the proposed 12T memory cell, if node pair S0–S1 is upset, transistors P7 and P8 will be temporarily turned OFF and ON, respectively. Subsequently, the analysis is the same as the analysis when the stored value of node S0 is changed. Therefore, nodes S0 and S1 will be pulled back to the original state, respectively.

5) Due to charge sharing effect, the voltage of node pair S0–QN or S1–QN can be changed, the stored state of the proposed 12T cell will be changed. Because both transistors P8 and N4 will be ON, and thus, node Q will be pulled down to state 0. This case is similar to a write 0 operation.

Therefore, when node S0 or S1 or QN or node pair S0–S1 in the proposed RHBD 12T cell is upset by a radiation particle, the stored data can be recovered from a corrupted data. When node pair S0–QN or S1–QN is upset, the stored data cannot be recovered. However, when the spacing of node QN and node pair S0–S1 is large enough, the possibilities of the multiple-node upset cases can be minimized. Fig. 3 shows the layout of the proposed 12T memory cell in which the transistors–transistor spacings of both node pairs S1–QN and S0–QN is greater than the effective range of charge sharing (about 1.5 μm [25], [26]). Therefore, in this paper, we focus only on the case when node pair S0–S1 is changed by a radiation particle.

III. Evaluations

A. SEU Tolerance Verification and Process Variation

In SEU fault injection simulations, the double current pulse source model [15] is employed to mimic the electronic effects of an SEU in a memory cell. Fig. 4(a) shows the fault injection equivalent circuit of a negative transient pulse, i.e., the drain terminal of the nMOS is connected to a double current pulse source to mimic a negative (1 → 0) transient pulse. Similarly, to generate a positive (0 → 1) transient pulse at the drain terminal of the pMOS, the current source model is also utilized again, as shown in Fig. 4(b). For multiple-node upset fault injection simulations, multiple current sources are applied to mimic the effects of charge sharing [16].

Using CMOS 65-nm twin well process, these memory cells are simulated at 1.2 V power supply and room temperature. Cadence Spectre simulations of nodes QN, S0, and S1 at the injected 70 fC charge are shown in Fig. 5(a)–(c), respectively. Evidently, it can be seen that when any one sensitive node is upset by a radiation particle, 12T memory cell can always recover to its right stored value. Therefore, the same as with cells RHD12T, DICE, R13T, 13T, and 11T, the proposed 12T memory cell can recover a 1 → 0 upset but also 0 → 1 upset. In other words, it can recover an SEU regardless of upset polarity. However, the obtained results simultaneously show that for the cells NS-10T, PS-10T, 10T, and 6T, they all are flipped and cannot recover to the initial value. Therefore, these cells cannot provide enough robustness of a single node upset. Fig. 5(d) shows that even though about 50 fC sharing charge is injected, the multiple-node upset at pair S0–S1 can also be tolerated. The comparison of radiation-induced critical charge in the primary affected node and the secondary affected node for these memory cells is clearly shown in Fig. 6. Critical charge Qcrit is the minimum charge that will be deposited at the sensitive node of a circuit to generate an SEU [15]. From Figs. 5(d) and 6, it can be seen that the proposed 12T and RHD12T cells have a better multiple-node upset robustness than other cells.

In semiconductor circuit manufacturing, process variation is the variation of fabrication process parameters in the attributes of transistors (e.g., length, widths, and oxide...
thickness) on a silicon wafer. Its effects can be predicated using Monte Carlo (MC) simulation in design stage. In accordance to the obtained MC results, designers can easily verify the variability of the designs before fabrication to determine whether they need to be revised and adjusted. MC simulation is successfully passed which means the design fabrication by foundry will be go a step further. In nanometer range, semiconductor circuits must confirm process variation effects that would potentially lead to the degradation of design performance. Therefore, in this paper, 1000 MC simulations (±5 Gaussian distribution with variation at the ±3σ level [16]) are also carried out to evaluate multiple-node upset robustness of these memory cells, and 40 fC charge is injected in primary and secondary affected nodes, respectively. MC simulations have confirmed that the proposed 12T memory cell can always recover to its normal state from a multiple-node upset, and node pair S0–S1 simulation result is chosen and shown in Fig. 7. Besides, for each memory cell, the failure probability of multiple-node upset is shown in Table I. It can be calculated by [16]

\[
\text{Failure probability} = \frac{\text{Number of flips}}{\text{Total number of simulations}}.
\]

As simulation results presented in Fig. 7 and Table I show, for the proposed RHBD 12T memory cell, process variation does not affect its multiple-node upset robustness. This is because that the proposed 12T memory cell has a better structure for tolerating a multiple-node upset. For the RHD12T cell, due to the STI approach, it can also tolerate a multiple-node upset. The other cells, such as 10T, 11T, and 13T, cannot recover from multiple-node upset, because their circuit structures enable them to only tolerate a single node upset.

### B. Comparisons of Cost and Robustness

The areas for various memory cells are shown and compared in Fig. 8. It provides evidences of the fact that the area of the proposed 12T memory cell is 85.5%, 93.8%, 95.2%, 81%, 94%, 117.9%, 102.6%, 107.9%, and 199.6% of cells R13T, RHD12T, DICE, 13T, 11T, PS-10T, NS-10T, 10T, and 6T, respectively. It should be noted that for R13T, 13T, and 11T cells, some refreshing and write select circuits must be added for providing the refreshing signals and generating the write-select signal, respectively, only in this way can memory timing and its fault robustness be executed rightly [15]–[17]. Therefore, these peripheral circuits together with memory arrays will be integrated into the memory. As a result, the area overhead of memory chip may be larger. Compared with 6T, 10T,
Table I

<table>
<thead>
<tr>
<th>Cell</th>
<th>Failure number</th>
<th>Failure probability</th>
<th>NS-10T</th>
<th>1000</th>
<th>100%</th>
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<tbody>
<tr>
<td>6T</td>
<td>1000</td>
<td>100%</td>
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<td></td>
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<tr>
<td>10T</td>
<td>1000</td>
<td>100%</td>
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<tr>
<td>PS-10T</td>
<td>1000</td>
<td>100%</td>
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<tr>
<td>NS-10T</td>
<td>1000</td>
<td>100%</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>11T</td>
<td>1000</td>
<td>100%</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>13T</td>
<td>1000</td>
<td>100%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DICE</td>
<td>1000</td>
<td>100%</td>
<td></td>
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<tr>
<td>RHD12T</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R13T</td>
<td>1000</td>
<td>100%</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>12T</td>
<td>0</td>
<td>0</td>
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</table>

NS-10T, and PS-10T cells, the proposed 12T memory cell has a larger area overhead. However, these memory cells cannot provide enough multiple-node upset robustness, as mentioned earlier.

To compare the robustness of these memory cells, soft error rate ratio (SERR) is also calculated by [27], [28]

\[
SERR = \frac{\sum_{i=1}^{n} P_{Ni} \cdot e^{-\beta \cdot Qcrit(i)}}{\sum_{j=1}^{n} P_{Nj} \cdot e^{-\beta \cdot Qcrit(j)}} (12T cell)
\]

where \(A_{Si}\) is the sensitive area of drain junctions of node \(i\), and \(A_{total}\) is the layout area of this memory cell. The sensitive area of the integrated circuit is the drain area of OFF transistors [1]. In the proposed 12T memory cell, the sensitive area of node QN is the drain area of pMOS transistor P2 plus the drain area of pMOS transistor P5. Therefore, the following values of \(A_{Si}\) can be presented: \(A_{S1} = 0.04845 \, \mu m^2\), \(A_{S2} = 0.0384 \, \mu m^2\), and \(A_{S3} = 0.0240 \, \mu m^2\).

In Table II, the SERR of various memory cells is compared. It shows the fact that although 6T cell has two sensitive nodes, it has the highest SERR value because of the lack of single node upset robustness in a sensitive node. Moreover, according to Table II and Fig. 6, an interesting phenomenon can be found is that a radiation hardened memory cell is not necessarily capable of tolerating a multiple-node upset when it can tolerate a single node upset. This can be proved by cells DICE, 13T, and R13T. For instance, although DICE cell can tolerate an SEU in a single node, it cannot tolerate multiple-node upset. Therefore, it has a higher SERR value compared with the proposed 12T memory cell. The 13T and R13T cells can also tolerate a single node upset, but the multiple-node upset tolerance capabilities of them are so weak that they have a higher SERR value. Compared with the proposed 12T cell, RHD12T cell also has a higher SERR value due to the increased sensitive area and the number of sensitive nodes (i.e., the number of its sensitive nodes is four, and the proposed 12T cell has only three sensitive nodes).
Fig. 9 shows the power consumption comparison of various memory cells. Fig. 9 provides evidences of the fact that the power consumption of the proposed 12T memory cell is smaller than the one of R13T, RHD12T, and 13T cells but larger than the one of other cells. The main reason for this is that, node QN is not 0 state (pMOS transistor can cause the threshold voltage degradation of 0 state); thus, nMOS transistor N4 is not turned OFF completely. As a result, there is a leakage path between VDD and GND through transistors P4, P8, and N4 so that its power consumption is increased.

In order to obtain read access time, a 0.2-pF capacitance is, respectively, connected to bit-lines BL and BLN to stimulate a high bitline capacity. Fig. 10 compares the read access times of these cells, and it shows that the read access times of other memory cells are smaller than that of the proposed 12T memory cell. Read access time strongly depends on the read current and the length of the read path. For the proposed 12T cell, in order to avoid a negative transient pulse induced by a radiation particle in Q and QN nodes, pMOS transistors (i.e., P2, P4, and P5–P8 transistors) are used. As a result, the driving voltages (or driving capabilities) of nodes Q and QN are reduced and the length of the read path is increased so that the read access time of the proposed 12T memory cell is increased.

Fig. 11 compares the write access times of different memory cells. As can be seen, the write access time of the proposed
12T cell is slightly larger than the one of 10T cell. The reduced driving capabilities of nodes Q and QN can decrease the degree of difficulty of writing data so that the write access time should be reduced. However, because of the increased feedback path length and node capacitances, its write access time is slightly increased.

C. Comparison of Stability

In memory designs, static noise margins (SNMs) are widely used as the criteria of stability. Here, read SNM (RSNM), write SNM (WSNM), and hold SNM margin (HSNM) of a memory cell are calculated, and the comparison result of various memory cells is shown in Fig. 12(a)–(c), respectively. In read case, because of the increased length of read path and the reduced driving voltages of nodes Q and QN, the proposed memory cell has a higher RSNM than the one of other cells except NS-10T cell. In write case, due to the same reason, the states of nodes Q and QN are more easily changed by write operations. Therefore, its WSNM is lower than the one of other memory cells. For the hold mode, the proposed RHBD 12T memory cell has the highest HSNM because of the increased length of feedback path. This result means that in the proposed RHBD 12T memory cell not only SEU robustness, but also a higher stability is simultaneously provided.

IV. CONCLUSION

In this paper, a novel 12T RHBD memory cell for mitigating soft error in 65-nm CMOS commercial technology is proposed. The main contribution of the proposed memory cell is that not only can it tolerate single node upset, but it can also provide effective multiple-node upset protection. 1000 MC simulations are also carried out, and the obtained simulation results clearly confirm that process variation does not affect its SEU robustness.

The shortcoming of the proposed 12T memory cell is its higher read access time which may have a negative impact on some high-speed applications. However, in critical aerospace applications, area, robustness, and reliability of memory may be more important. Hence, from a critical application designer point of view, the RHBD 12T memory cell proposed in this paper is a good design for radiation robustness compared with other state-of-the-art hardened memory cells. Therefore, the trend of this paper is to continually optimize its time performance and reduce its area overhead.

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circuits.
reliability in spin-transfer torque magnetoresistive random-access memory


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