Novel Radiation-Hardened-by-Design (RHBD) 12T Memory Cell for Aerospace Applications in Nanoscale CMOS Technology

Jing Guo, Lei Zhu, Wenyi Liu, Hai Huang, Shanshan Liu, Tianqi Wang, Liyi Xiao, *Member, IEEE*, and Zhigang Mao

***Abstract*— In this paper, a novel radiation-hardened-by-design (RHBD) 12T memory cell is proposed to tolerate single node upset and multiple-node upset based on upset physical mechanism behind soft errors together with reasonable layout-topology. The verification results obtained confirm that the proposed 12T cell can provide a good radiation robustness. Compared with 13T cell, the increased area, power, read/write access time overheads of the proposed 12T cell are −18.9%, −23.8%, and 171.6%/−50.0%, respectively. Moreover, its hold static noise margin is 986.2 mV which is higher than that of 13T cell. This means that the proposed 12T cell also has higher stability when it provides fault tolerance capability.**

***Index Terms*— Memory, multiple-node upset, radiation-hardened-by-design (RHBD), soft errors.**

I. Introduction

MEMORIES are extensively used in aerospace applications as the medium to store data in which single event upsets (SEUs) induced by radiation particles are becoming one of the most significant issues [1]–[5]. Because they can conduce to the data corruption in a memory chip and the circuit itself is not permanently damaged, SEUs are also described as the soft errors [1]. Therefore, SEUs can cause a malfunctioning of an electronic system. In some critical memory applications (e.g., satellite equipment [5], [6] and cardioverter defibrillators [7]), SEUs can be detrimental and crucial. However, radiation hardening techniques for memories are one of the bottlenecks in providing fault tolerance.

For many years, some radiation-hardening-by-design (RHBD) techniques have been used to tolerate soft errors in memories using standard commercial CMOS foundry processes, with no modifications to the existing process or violation of design rules [6]. Traditionally, these techniques can be mainly divided into the following three subitem techniques.

1) Layout-level techniques employ mainly layout changes, such as H-gate, T-gate, annular-gate, and shallow trench isolation (STI) for the radiation tolerance [8], [9]. Although it is generally true that these layout-level techniques do provide partial protection capability, they are difficult to implement in nanometer technologies due to more exigent design rules.
2) The first circuit-level technique is triple modular redundancy (TMR) which is used for mitigating SEU in memories or latches [10]. This hardening technique relies on three copies of memory cell to store the same data, and a voting circuitry to determine the right output. If one cell is upset, the remaining two copies still remain unchanged from the initial data. Then, the voting is executed by the majority voting process so that the stored data can be output rightly. The main issue of TMR is that it has to incur a large area overhead and power dissipation [11]. The most common circuit-level hardening techniques are to add extra redundant transistors based on standard 6T cell or to propose new hardened memory cells. For example, Jahinuzzaman *et al.* [12], have proposed a 10T hardened memory cell using ten transistors. However, it can only recover $1 \rightarrow 0$ SEU. In [13], PS-10T and NS-10T hardened memory cells are proposed to provide only partial SEU robustness. In others words, PS-10T cell can only recover $1 \rightarrow 0$ SEU and NS-10T cell is only capable of recovering $0 \rightarrow 1$ SEU. In [14], the dual interlocked storage cell (DICE) is proposed, which utilizes 12 transistors to obtain fault robustness in any one single node. Recently, 11T and 13T cells are, respectively, proposed in [15] and [16] using single-ended memory structure. Compared with 11T cell, the sharing critical charge of 13T cell is slightly increased due to the hysteresis effect of the Schmitt trigger. Rajaei *et al.* [17] have optimized

Manuscript received August 14, 2016; revised October 24, 2016 and December 20, 2016; accepted December 21, 2016. This work was supported in part by the National Natural Science Foundation of China under Grant 61604133 and Grant 61501275, in part by the Science Foundation of North University of China under Grant 110248-29140, and in part by the Science Foundation Project of Heilongjiang Province of China under Grant QC2015073.

J. Guo and W. Liu are with the Science and Technology on Electronic Test and Measurement Laboratory, and the Key Laboratory of Instrumentation Science and Dynamic Measurement, Ministry of Education, North University of China, Taiyuan 030051, China (e-mail: guojing19861229@163.com).

L. Zhu is with the Communication and Electronics Engineering Institute, Qiqihar University, Qiqihar 161006, China.

H. Huang is with the School of Software, Harbin University of Science and Technology, Harbin 150001, China, and also with the Institute of Microelectronics, Tsinghua University, Beijing 100084, China.

S. Liu, T. Wang, and L. Xiao are with the Microelectronics Center, Harbin Institute of Technology, Harbin 150001, China.

Z. Mao was with the Microelectronics Center, Harbin Institute of Technology, Harbin 150001, China. He is now with the School of Microelectronics, Shanghai Jiao Tong University, Shanghai 200240, China.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TVLSI.2016.2645282

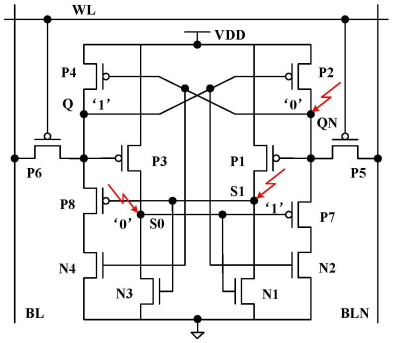


Fig. 1. Proposed RHBD 12T memory cell.

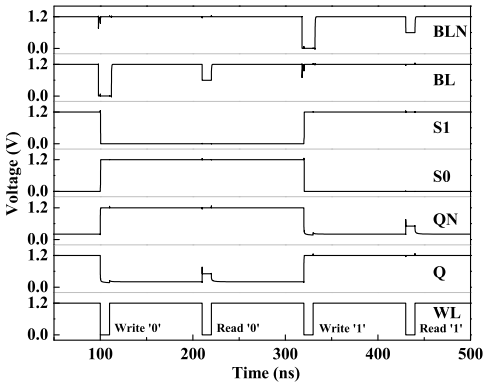


Fig. 2. Transient simulation result of the proposed RHBD 12T cell.

the structure of 13T memory cell to propose a new hardened memory cell (R13T). Compared with 13T cell, R13T cell has more shared critical charge. However, the main drawback of these cells is that they cannot tolerate a multiple-node upset. In [9], by using circuit-level hardening technique together with layout-level STI approach, an RHD12T memory cell is proposed to tolerate a multiple-node upset. However, this memory cell has more area overhead and lower stability.

3) System-level techniques mean that they utilize some error detection and correction codes (ECCs) to tolerate soft errors at the system-level architecture [18]–[20]. However, ECC techniques would require more overheads especially for time performance (nanosecond-level delay), since the encoding and decoding circuits are more complex [21]–[24]. This means that the time performance of memory will be affected severely.

In general, compared with layout- and system-level hardening techniques, the advantage of circuit-level RHBD memory design is that it can provide not only higher fault tolerate capability, but also lower overheads especially for time performance (picosecond-level delay). Therefore, in this paper, we focus on proposing a novel circuit-level RHBD 12T cell to improve the SEU robustness of memories.

The remainder of this paper is mainly divided into the following sections. Section II introduces the proposed RHBD 12T cell structure, write/read timing, and SEU recovery analysis. In Section III, the SEU recovery simulations, and the detailed performance comparisons for various memory cells are shown. Finally, some conclusions are presented in Section IV.

II. RHBD 12T Memory Cell Design

A. Cell Schematic and Write/Read Timing

The proposed RHBD 12T memory cell is shown in Fig. 1. Here, two access transistors, pMOS transistors P5 and P6, have been connected bit-lines BLN and BL to the output nodes QN and Q, respectively. Their ON/OFF state is determined by a word-line WL. It should be noted that when a radiation particle strikes pMOS transistor, only a positive transient pulse (0→1 or 1 → 1 transient pulse) can be generated; on the contrary, only a negative transient pulse (1 → 0 or 0→0 transient pulse) can be induced when a radiation particle strikes nMOS transistor [2]. Therefore, in order to avoid a negative transient pulse induced by a radiation particle in Q and QN nodes, pMOS transistors (i.e., transistors P6 and P5) are used as access transistors.

Considering the stored 1 state (i.e., QN = 0, Q = 1, $S0$ = 0, and $S1$ = 1) for the proposed RHBD 12T cell (see Fig. 1).

1) When word-line WL is high state 1, transistors P1, P4, P7, N2, and N3 are ON, and the remaining transistors are OFF. Thus, nodes Q and QN are not changed, and they also stored their original data, respectively.
2) Before read operation is executed in the proposed 12T memory cell, two bit-lines BL and BLN need to be precharged to supply voltage VDD. After read operation, and word-line WL is 0 state, the output node Q will store its original state 1 without changing. However, because transistors P5, P7, and N2 are ON, bitline BLN will be discharged. Next, when the voltage difference between two bit-lines BL and BLN are obtained, the differential sense amplifier in memories will output the stored data.
3) To write data 0 into the proposed 12T cell, word-line WL and bitline BL need to be 0 state, and bitline BLN must be 1 state. Subsequently, node Q will be pulled down to 0 state, and node QN will be pulled up to 1 state. Transistors P2, P3, P8, N1, and N4 will be ON, and transistors P1, P4, P7, N2, and N3 will be OFF. When word-line WL is pulled back to high state 1, the stored data will be 0. This means that data 0 can be successfully written into the proposed RHBD 12T memory cell.

Fig. 2 shows a "write 0, read 0, write 1, and read 1" transient simulation result. From Fig. 2, we can see that the proposed cell can rightly achieve write and read operations.

B. SEU Recovery Analysis

In this section, the SEU recovery analysis results for the proposed RHBD 12T memory cell are presented. Considering the state shown in Fig. 1, node Q is not a sensitive node, because it is connected with the drain area of OFF pMOS transistors P6 and P8, and its stored value is 1 state. Therefore, according to the upset physical mechanism, when node Q is strike, only a positive pulse is induced, i.e., node Q will be affected by a 1 → 1 transient pulse so that the stored value of node Q is not changed.

1) When node QN is upset by a radiation particle, node QN will be pulled up to state 1, then transistors P1 and P4 will be OFF. Subsequently, nodes Q and S1 will remain the original logic 1 state without losing voltage value. Therefore, transistor N3 will not be OFF, and node S0 keeps its original 0 state. Transistor P7 and N2 will be ON state, and then, node QN will be pulled back to its original state 0.
2) When a radiation particle strikes node S0, its value will be changed. Then, transistor P7 is temporarily turned OFF, and transistor N1 is temporarily turned ON, and thus, node S1 will be pulled down to 0. However, because of capacitive effect, node QN will not be changed to 1 state, and transistors N4 and P1 keep their OFF and ON states, respectively. Therefore, node Q will be unchanged through ON transistor P4, and node S1 can recover to initial 1 state. Finally, transistor N3 are turned ON, and node S0 will be pulled back to its original 0 state.
3) When the state of node S1 is changed to 0 from original 1 state by a radiation particle, transistors N3 and P8 will be turned OFF and ON, respectively. Because the voltages of nodes Q, QN, and S0 will be unchanged, transistor P1 remains ON. Therefore, node S1 will be pulled back to its original 1 state through ON transistor P1.
4) When a radiation particle strikes a semiconductor device because of charge sharing effect, multiple sensitive nodes may be affected. In the proposed 12T memory cell, if node pair S0–S1 is upset, transistors P7 and P8 will be temporarily turned OFF and ON, respectively. Subsequently, the analysis is the same as the analysis when the stored value of node S0 is changed. Therefore, nodes S0 and S1 will be pulled back to the original state, respectively.
5) Due to charge sharing effect, the voltage of node pair S0–QN or S1–QN can be changed, the stored state of the proposed 12T cell will be changed. Because both transistors P8 and N4 will be ON, and thus, node Q will be pulled down to state 0. This case is similar to a write 0 operation.

Therefore, when node S0 or S1 or QN or node pair S0–S1 in the proposed RHBD 12T cell is upset by a radiation particle, the stored data can be recovered from a corrupted data. When node pair S0–QN or S1–QN is upset, the stored data cannot be recovered. However, when the spacing of node QN and node pair S0–S1 is large enough, the possibilities of the multiple-node upset cases can be minimized. Fig. 3 shows the layout of the proposed 12T memory cell in which the transistors–transistor spacings of both node pairs S1–QN and S0–QN is greater than the effective range of charge sharing (about 1.5 μm [25], [26]). Therefore, in this paper, we focus only on the case when node pair S0–S1 is changed by a radiation particle.

III. Evaluations

A. SEU Tolerance Verification and Process Variation

In SEU fault injection simulations, the double current pulse source model [15] is employed to mimic the electronic effects

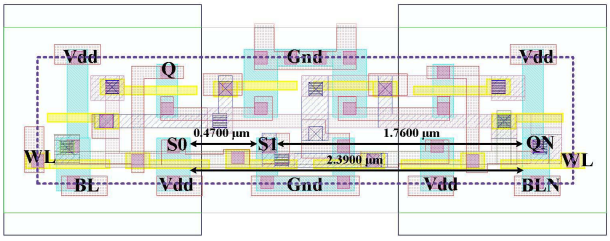


Fig. 3. Layout of the proposed RHBD 12T cell (area = 0.8950 × 3.8850 = 3.4502 μm^2).

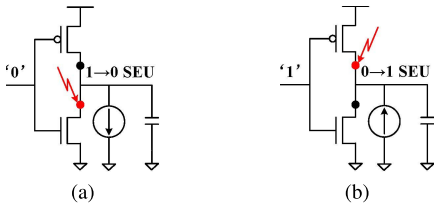


Fig. 4. Fault injection equivalent circuits. (a) Negative transient pulse is used to mimic a 1 → 0 SEU. (b) Positive transient pulse is used to mimic a 0→1 SEU.

of an SEU in a memory cell. Fig. 4(a) shows the fault injection equivalent circuit of a negative transient pulse, i.e., the drain terminal of the nMOS is connected to a double current pulse source to mimic a negative (1 → 0) transient pulse. Similarly, to generate a positive (0 →1) transient pulse at the drain terminal of the pMOS, the current source model is also utilized again, as shown in Fig. 4(b). For multiple-node upset fault injection simulations, multiple current sources are applied to mimic the effects of charge sharing [16].

Using CMOS 65-nm twin well process, these memory cells are simulated at 1.2 V power supply and room temperature. Cadence Spectre simulations of nodes QN, S0, and S1 at the injected 70 fC charge are shown in Fig. 5(a)–(c), respectively. Evidently, it can be seen that when any one sensitive node is upset by a radiation particle, 12T memory cell can always recover to its right stored value. Therefore, the same as with cells RHD12T, DICE, R13T, 13T, and 11T, the proposed 12T memory cell can recover a 1 → 0 upset but also 0 →1 upset. In other words, it can recover an SEU regardless of upset polarity. However, the obtained results simultaneously show that for the cells NS-10T, PS-10T, 10T, and 6T, they all are flipped and cannot recover to the initial value. Therefore, these cells cannot provide enough robustness of a single node upset. Fig. 5(d) shows that even though about 50 fC sharing charge is injected, the multiple-node upset at pair S0–S1 can also be tolerated. The comparison of radiation-induced critical charge in the primary affected node and the secondary affected node for these memory cells is clearly shown in Fig. 6. Critical charge Q_{crit} is the minimum charge that will be deposited at the sensitive node of a circuit to generate an SEU [15]. From Figs. 5(d) and 6, it can be seen that the proposed 12T and RHD12T cells have a better multiple-node upset robustness than other cells.

In semiconductor circuit manufacturing, process variation is the variation of fabrication process parameters in the attributes of transistors (e.g., length, widths, and oxide

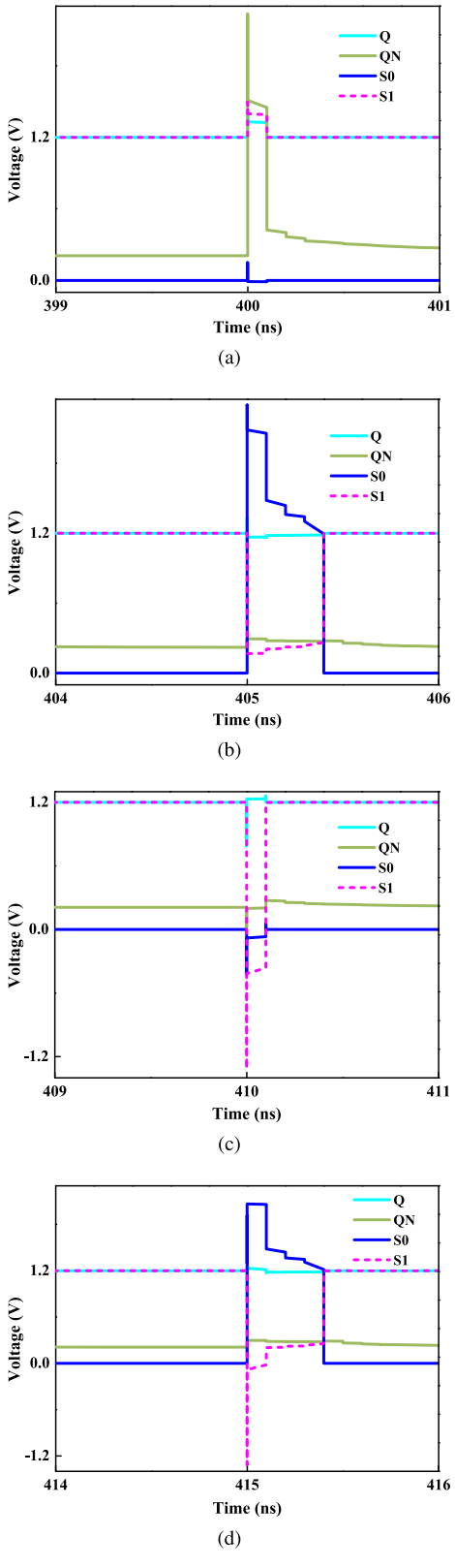


Fig. 5. Fault injection simulation waveforms. (a) Node QN is upset. (b) Node S0 is upset. (c) Node S1 is upset. (d) Node pair S0–S1 is upset.

thickness) on a silicon wafer. Its effects can be predicated using Monte Carlo (MC) simulation in design stage. In accordance to the obtained MC results, designers can easily verify the variability of the designs before fabrication to determine whether they need to be revised and adjusted. MC simulation is successfully passed which means the design fabrication by foundry will be go a step further. In nanometer range, semiconductor circuits must confirm process variation effects that would potentially lead to the degradation of design performance. Therefore, in this paper, 1000 MC simulations (±5 Gaussian distribution with variation at the $\pm 3\sigma$ level [16]) are also carried out to evaluate multiple-node upset robustness of these memory cells, and 40 fC charge is injected in primary and secondary affected nodes, respectively. MC simulations have confirmed that the proposed 12T memory cell can always recover to its normal state from a multiple-node upset, and node pair S0–S1 simulation result is chosen and shown in Fig. 7. Besides, for each memory cell, the failure probability of multiple-node upset is shown in Table I. It can be calculated by [16]

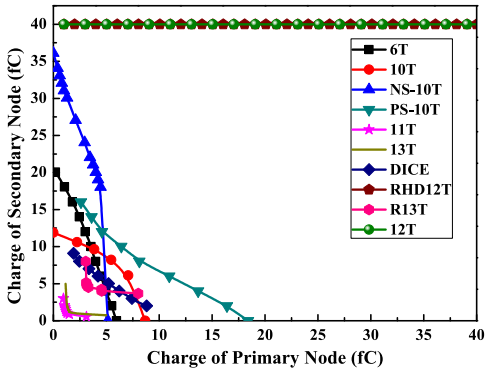


Fig. 6. Critical charge comparison in the primary and secondary nodes for the different cells.

$$\text{Failure probability} = \frac{\text{Number of flips}}{\text{Total number of simulations}}. \quad (1)$$

As simulation results presented in Fig. 7 and Table I show, for the proposed RHBD 12T memory cell, process variation does not affect its multiple-node upset robustness. This is because that the proposed 12T memory cell has a better structure for tolerating a multiple-node upset. For the RHD12T cell, due to the STI approach, it can also tolerate a multiple-node upset. The other cells, such as 10T, 11T, and 13T, cannot recover from multiple-node upset, because their circuit structures enable them to only tolerate a single node upset.

B. Comparisons of Cost and Robustness

The areas for various memory cells are shown and compared in Fig. 8. It provides evidences of the fact that the area of the proposed 12T memory cell is 85.5%, 93.8%, 95.2%, 81%, 94%, 117.9%, 102.6%, 107.9%, and 199.6% of cells R13T, RHD12T, DICE, 13T, 11T, PS-10T, NS-10T, 10T, and 6T, respectively. It should be noted that for R13T, 13T, and 11T cells, some refreshing and write select circuits must be added for providing the refreshing signals and generating the write-select signal, respectively, only in this way can memory timing and its fault robustness be executed rightly [15]–[17]. Therefore, these peripheral circuits together with memory arrays will be integrated into the memory. As a result, the area overhead of memory chip may be larger. Compared with 6T, 10T,

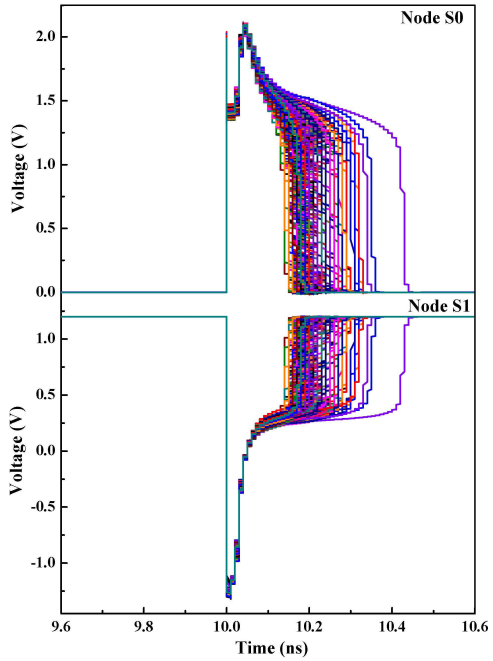


Fig. 7. 1000 MC simulation waveform of node pair S0–S1.

TABLE I
FAILURE PROBABILITY FOR EACH MEMORY CELL

Cell	Failure number	Failure probability
6T	1000	100%
10T	1000	100%
PS-10T	1000	100%
NS-10T	1000	100%
11T	1000	100%
13T	1000	100%
DICE	1000	100%
RHD12T	0	0
R13T	1000	100%
12T	0	0

NS-10T, and PS-10T cells, the proposed 12T memory cell has a larger area overhead. However, these memory cells cannot provide enough multiple-node upset robustness, as mentioned earlier.

To compare the robustness of these memory cells, soft error rate ratio (SERR) is also calculated by [27], [28]

$$\text{SERR} = \frac{\sum_{i=1}^{n} P_{Ni} \cdot \alpha \cdot e^{-\beta \cdot Q_{crit}(i)}(\text{comp\_cell})}{\sum_{j=1}^{n} P_{Nj} \cdot \alpha \cdot e^{-\beta \cdot Q_{crit}(j)}(\text{12T cell})} \tag{2}$$

where α and β are fitting parameters which depend on process technology node, and P_{Ni} is the probability that a sensitive node of a memory cell is affected by a radiation particle. It should be noted that in the same process technology node, α and β are the same for all compared memory cells. Higher P_{Ni} means higher possibility to be affected for a memory cell, and it can be directly obtained by [27], [28]

$$P_{Ni} = \frac{A_{Si}}{A_{\text{total}}} \tag{3}$$

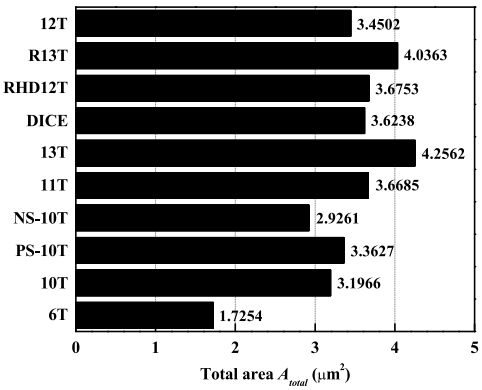


Fig. 8. Comparison of area for the different cells.

TABLE II
SERR COMPARISON OF VARIOUS MEMORY CELLS

Cell	SERR	Number of sensitive nodes
6T	102.7269	2
10T	16.1039	4
PS-10T	20.5257	4
NS-10T	92.2047	4
11T	90.6658	4
13T	61.6335	4
DICE	39.8489	4
RHD12T	2.1895	4
R13T	51.4123	4
12T	1	3

where A_{Si} is the sensitive area of drain junctions of node i, and A_{total} is the layout area of this memory cell. The sensitive area of the integrated circuit is the drain area of OFF transistors [1]. In the proposed 12T memory cell, the sensitive area of node QN is the drain area of pMOS transistor P2 plus the drain area of pMOS transistor P5. Therefore, the following values of A_{Si} can be presented: $A_{S1} = 0.04845\ \mu m^2$, $A_{S2} = 0.0384\ \mu m^2$, and $A_{S3} = 0.0240\ \mu m^2$.

In Table II, the SERR of various memory cells is compared. It shows the fact that although 6T cell has two sensitive nodes, it has the highest SERR value because of the lack of single node upset robustness in a sensitive node. Moreover, according to Table II and Fig. 6, an interesting phenomenon can be found is that a radiation hardened memory cell is not necessarily capable of tolerating a multiple-node upset when it can tolerate a single node upset. This can be proved by cells DICE, 13T, and R13T. For instance, although DICE cell can tolerate an SEU in a single node, it cannot tolerate multiple-node upset. Therefore, it has a higher SERR value compared with the proposed 12T memory cell. The 13T and R13T cells can also tolerate a single node upset, but the multiple-node upset tolerance capabilities of them are so weak that they have a higher SERR value. Compared with the proposed 12T cell, RHD12T cell also has a higher SERR value due to the increased sensitive area and the number of sensitive nodes (i.e., the number of its sensitive nodes is four, and the proposed 12T cell has only three sensitive nodes).

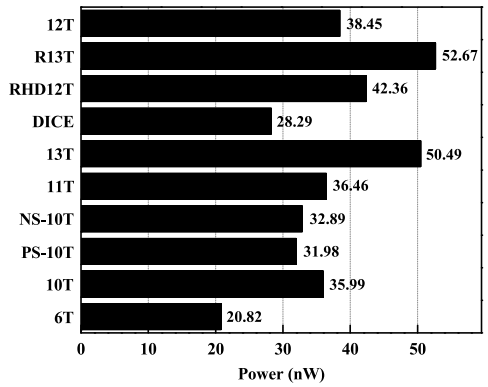


Fig. 9. Power comparison of the different cells.

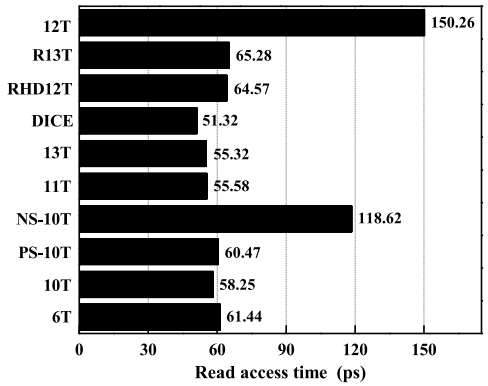


Fig. 10. Comparison of read access time for the different cells.

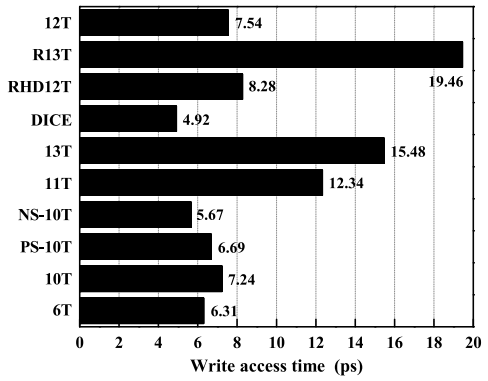


Fig. 11. Comparison of write access time for the different cells.

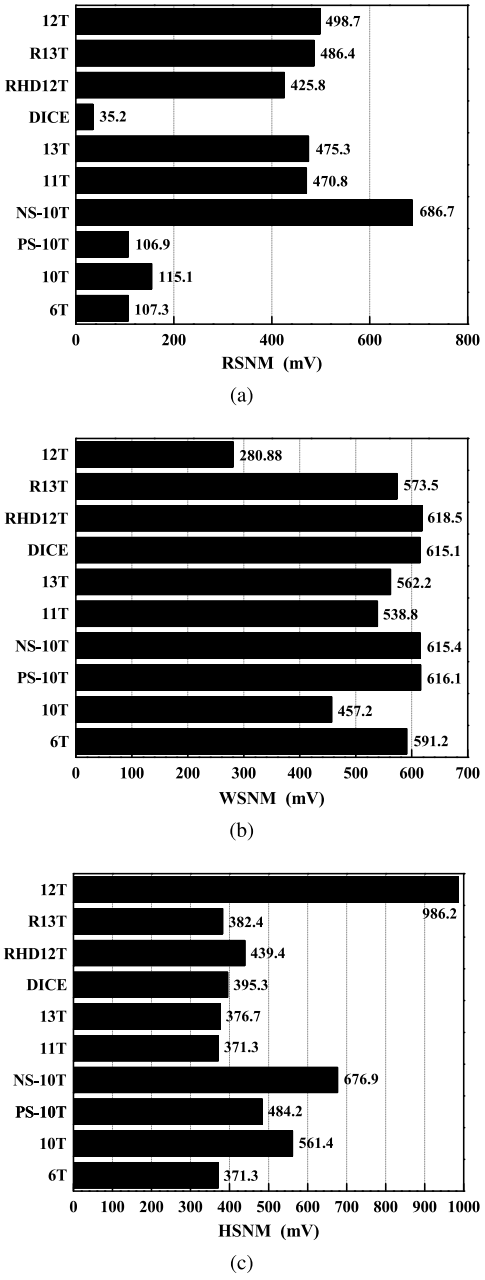


Fig. 12. Comparison of SNM for various cells. (a) RSNM. (b) WSNM. (c) HSNM.

Fig. 9 shows the power consumption comparison of various memory cells. Fig. 9 provides evidences of the fact that the power consumption of the proposed 12T memory cell is smaller than the one of R13T, RHD12T, and 13T cells but larger than the one of other cells. The main reason for this is that, node QN is not 0 state (pMOS transistor can cause the threshold voltage degradation of 0 state); thus, nMOS transistor N4 is not turned OFF completely. As a result, there is a leakage path between VDD and GND through transistors P4, P8, and N4 so that its power consumption is increased.

In order to obtain read access time, a 0.2-pF capacitance is, respectively, connected to bit-lines BL and BLN to stimulate a high bitline capacity. Fig. 10 compares the read access times of these cells, and it shows that the read access times of other memory cells are smaller than that of the proposed 12T memory cell. Read access time strongly depends on the read current and the length of the read path. For the proposed 12T cell, in order to avoid a negative transient pulse induced by a radiation particle in Q and QN nodes, pMOS transistors (i.e., P2, P4, and P5–P8 transistors) are used. As a result, the driving voltages (or driving capabilities) of nodes Q and QN are reduced and the length of the read path is increased so that the read access time of the proposed 12T memory cell is increased.

Fig. 11 compares the write access times of different memory cells. As can be seen, the write access time of the proposed

12T cell is slightly larger than the one of 10T cell. The reduced driving capabilities of nodes Q and QN can decrease the degree of difficulty of writing data so that the write access time should be reduced. However, because of the increased feedback path length and node capacitances, its write access time is slightly increased.

C. Comparison of Stability

In memory designs, static noise margins (SNMs) are widely used as the criteria of stability. Here, read SNM (RSNM), write SNM (WSNM), and hold SNM margin (HSNM) of a memory cell are calculated, and the comparison result of various memory cells is shown in Fig. 12(a)–(c), respectively. In read case, because of the increased length of read path and the reduced driving voltages of nodes Q and QN, the proposed memory cell has a higher RSNM than the one of other cells except NS-10T cell. In write case, due to the same reason, the states of nodes Q and QN are more easily changed by write operations. Therefore, its WSNM is lower than the one of other memory cells. For the hold mode, the proposed RHBD 12T memory cell has the highest HSNM because of the increased length of feedback path. This result means that in the proposed RHBD 12T memory cell not only SEU robustness, but also a higher stability is simultaneously provided.

IV. Conclusion

In this paper, a novel 12T RHBD memory cell for mitigating soft error in 65-nm CMOS commercial technology is proposed. The main contribution of the proposed memory cell is that not only can it tolerate single node upset, but it can also provide effective multiple-node upset protection. 1000 MC simulations are also carried out, and the obtained simulation results clearly confirm that process variation does not affect its SEU robustness.

The shortcoming of the proposed 12T memory cell is its higher read access time which may have a negative impact on some high-speed applications. However, in critical aerospace applications, area, robustness, and reliability of memory may be more important. Hence, from a critical application designer point of view, the RHBD 12T memory cell proposed in this paper is a good design for radiation robustness compared with other state-of-the-art hardened memory cells. Therefore, the trend of this paper is to continually optimize its time performance and reduce its area overhead.

References

[1] E. Ibe, H. Taniguchi, Y. Yahagi, K.-I. Shimbo, and T. Toba, "Impact of scaling on neutron-induced soft error in SRAMs from a 250 nm to a 22 nm design rule," *IEEE Trans. Electron Devices*, vol. 57, no. 7, pp. 1527–1538, Jul. 2010.

[2] P. E. Dodd and L. W. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 583–602, Jun. 2003.

[3] R. C. Baumann, "Soft errors in advanced semiconductor devices part I: The three radiation sources," *IEEE Trans. Device Mater. Rel.*, vol. 1, no. 1, pp. 17–22, Mar. 2001.

[4] H. L. Hughes and J. M. Benedetto, "Radiation effects and hardening of MOS technology: Devices and circuits," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 500–521, Jun. 2003.

[5] C. Boatella, G. Hubert, R. Ecoffet, and S. Duzellier, "ICARE on-board SAC-C: More than 8 years of SEU and MCU, analysis and prediction," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 4, pp. 2000–2009, Aug. 2003.

[6] Y. Bentoutou, "A real time EDAC system for applications onboard earth observation small satellites," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 48, no. 1, pp. 648–657, Jan. 2012.

[7] P. D. Bradley and E. Normand, "Single event upsets in implantable cardioverter defibrillators," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, pp. 2929–2940, Dec. 1998.

[8] M. L. McLain, H. J. Barnaby, I. S. Esqueda, J. Oder, and B. Vermeire, "Reliability of high performance standard two-edge and radiation hardened by design enclosed geometry transistors," in *Proc. IEEE Int. Rel. Phys. Symp.*, Apr. 2009, pp. 174–179.

[9] C. Qi, L. Xiao, T. Wang, J. Li, and L. Li, "A highly reliable memory cell design combined with layout-level approach to tolerant single-event upsets," *IEEE Trans. Device Mater. Rel.*, vol. 16, no. 3, pp. 388–395, Sep. 2016.

[10] D. R. Blum and J. G. Delgado-Frias, "Schemes for eliminating transient-width clock overhead from SET-tolerant memory-based systems," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 3, pp. 1564–1573, Jun. 2006.

[11] S.-F. Liu, P. Reviriego, and J. A. Maestro, "Efficient majority logic fault detection with difference-set codes for memory applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 1, pp. 148–156, Jan. 2012.

[12] S. M. Jahinuzzaman, D. J. Rennie, and M. Sachdev, "A soft error tolerant 10T SRAM bit-cell with differential read capability," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3768–3773, Dec. 2009.

[13] I.-S. Jung, Y.-B. Kim, and F. Lombardi, "A novel sort error hardened 10T SRAM cells for low voltage operation," in *Proc. IEEE 55th Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2012, pp. 714–717.

[14] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 6, pp. 2874–2878, Dec. 1996.

[15] S. Lin, Y.-B. Kim, and F. Lombardi, "A 11-transistor nanoscale CMOS memory cell for hardening to soft errors," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 5, pp. 900–904, May 2012.

[16] S. Lin, Y.-B. Kim, and F. Lombardi, "Analysis and design of nanoscale CMOS storage elements for single-event hardening with multiple-node upset," *IEEE Trans. Device Mater. Rel.*, vol. 12, no. 1, pp. 68–77, Mar. 2012.

[17] R. Rajaei, B. Asgari, M. Tabandeh, and M. Fazeli, "Design of robust SRAM cells against single-event multiple effects for nanometer technologies," *IEEE Trans. Device Mater. Rel.*, vol. 15, no. 3, pp. 429–436, Sep. 2015.

[18] P. Reviriego, J. A. Maestro, and M. F. Flanagan, "Error detection in majority logic decoding of Euclidean geometry low density parity check (EG-LDPC) codes," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 21, no. 1, pp. 156–159, Jan. 2013.

[19] J. Guo, L. Xiao, Z. Mao, and Q. Zhao, "Enhanced memory reliability against multiple cell upsets using decimal matrix code," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 1, pp. 127–135, Jan. 2014.

[20] R. Naseer and J. Draper, "Parallel double error correcting code design to mitigate multi-bit upsets in SRAMs," in *Proc. 34th Eur. Solid-State Circuits*, Sep. 2008, pp. 222–225.

[21] C. Yang, Y. Emre, and C. Chakrabarti, "Product code schemes for error correction in MLC NAND flash memories," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 12, pp. 2302–2314, Dec. 2012.

[22] H. Naeimi and A. DeHon, "Fault secure encoder and decoder for nanomemory applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, no. 4, pp. 473–486, Apr. 2009.

[23] P. Reviriego, M. F. Flanagan, S.-F. Liu, and J. A. Maestro, "Multiple cell upset correction in memories using difference set codes," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 11, pp. 2592–2599, Nov. 2012.

[24] P. Reviriego, S. Pontarelli, and J. A. Maestro, "Concurrent error detection for orthogonal latin squares encoders and syndrome computation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 21, no. 12, pp. 2334–2338, Dec. 2013.

[25] R. Harada, Y. Mitsuyama, M. Hashimoto, and T. Onoye, "Neutron induced single event multiple transients with voltage scaling and body biasing," in *Proc. IEEE IRPS*, Apr. 2011, pp. 3C.4.1–3C.4.5.

[26] O. A. Amusan *et al.*, "Charge collection and charge sharing in a 130 nm CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3253–3258, Dec. 2006.

[27] H. Nan and K. Choi, "High performance, low cost, and robust soft error tolerant latch designs for nanoscale CMOS technology," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 7, pp. 1445–1457, Jul. 2012.
[28] M. Omana, D. Rossi, and C. Metra, "High-performance robust latches," *IEEE Trans. Comput.*, vol. 59, no. 11, pp. 1455–1465, Nov. 2010.

Jing Guo received the B.S. and M.S. degrees in electronic science and technology from Heilongjiang University, Harbin, China, in 2008 and 2011, respectively, and the Ph.D. degree in microelectronics and solid-state electronics from the Harbin Institute of Technology, Harbin, in 2015.

He is currently a Lecturer with the National Key Laboratory for Electronic Measurement Technology, and the Key Laboratory of Instrumentation Science and Dynamic Measurement, North University of China, Taiyuan, China. His current research interests include fault tolerance in VLSI designs and reliability in memories.

Dr. Guo is the author of four technical papers in the IEEE Journals, including the IEEE TRANSACTIONS ON VLSI, the IEEE TRANSACTIONS ON RELIABILITY, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS, and the IEEE MICRO. He is also the co-author of over two technical papers in the IEEE TRANSACTIONS ON NUCLEAR SCIENCE, and *Microelectronics Reliability*.

Lei Zhu received the B.S. degree in communication engineering and the M.S. degree in communication and information system from Qiqihar University, Qiqihar, China, in 2004 and 2010, respectively, and the Ph.D. degree in electronic science and technology from the Harbin Institute of Technology, Harbin, China, in 2015.

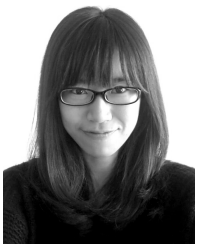
Since 2004, she has been with the Communication and Electronics Engineering Institute, Qiqihar University, where she is currently an Associate Professor. She has published over 20 international and regional refereed journal papers. Her current research interests include electromagnetic, optical metamaterials, microwave devices, RF circuits, and reliability in spin-transfer torque magnetoresistive random-access memory circuits.

Wenyi Liu received the B.S. degree in safety engineering, the M.S. degree in computer software, and the Ph.D. degree in instrument science and technology from the North University of China, Taiyuan, China, in 1992, 1998, and 2009, respectively.

Since 2009, he has been a Professor with the North University of China. He served as a Visiting Scientist with the College of Engineering, Design and Physical Sciences, Brunel University, London, U.K., in 2013. His current research interests include digital signal processing, compression coding, storage testing, and embedded systems.

Hai Huang received the B.S. and M.S. degrees in control theory and control engineering from the Harbin University of Science and Technology, Harbin, China, in 2004 and 2007, respectively, and the Ph.D. degree in microelectronics and solid state electronics from the Harbin Institute of Technology, Harbin, in 2013.

Since 2014, he has been an Associate Professor with the School of Software, Harbin University of Science and Technology. He is currently a Post-Doctoral Research Fellow with the Institute of Microelectronics, Tsinghua University, Beijing, China. His current research interests include information security, reconfigurable computing, and VLSI DSP.



Shanshan Liu received the B.S. degree in electronic science and technology from the Harbin University of Science and Technology, Harbin, China, in 2012, and the M.S. degree in microelectronics and solid-state electronics from the Harbin Institute of Technology, Harbin, in 2012, where she is currently pursuing the Ph.D. degree in microelectronics and solid-state electronics.

Her current research interests include fault tolerance in VLSI designs and reliability in memories.

Tianqi Wang received the B.E. and M.S. degrees from Heilongjiang University, Harbin, China, in 2006 and 2010, respectively, and the Ph.D. degree in electronic science and technology from the Harbin Institute of Technology, Harbin, in 2016.

He is currently a Lecturer with the Harbin Institute of Technology. His current research interests include the effects of radiation on integrated circuits and the radiation hardening by design techniques.

Liyi Xiao (M'07) received the B.S., M.S., and Ph.D. degrees from the Harbin Institute of Technology, Harbin, China, in 1984, 1989, and 2001, respectively, all in microelectronics and solid-state electronics.

Her current research interests include reliability in semiconductor devices and extra-low power design in VLSI, ASIC/SoC.

Zhigang Mao received the B.S. degree in semiconductor devices and physics from Tsinghua University, Beijing, China, in 1986, the M.S. degree from SUPELEC, Gif-sur-Yvette, France, in 1988, and the Ph.D. degree in information and communication from the University de Rennes I, Rennes, France, in 1992.

From 1992 to 2006, he was a Professor with the Harbin Institute of Technology, Harbin, China. He was the Main Designer of the first IC Card Chip in China. He is currently the Dean of the School of Microelectronics with Shanghai Jiao Tong University, Shanghai, China. His current research interests include VLSI design methodology, high-speed digital circuit design technology, low power electronics, signal processor architecture, and hardware security technology and reliability in semiconductor devices.

Dr. Mao has received the National Award for Science and Technology Progress, and two Province Awards for Science and Technology Progress.