# An Approach of Hybrid Modulation in Fusion seven-level Cascaded Multilevel Inverter accomplishment to IM drive system

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**Abstract— A new modulation topology of seven level cascaded multilevel inverter fed with induction motor drive system with considerable reduction of semiconductors switches and DC voltage sources has been developed. In recent day's Multilevel inverter (MLI) technologies become an incredible main choice in the area of high power medium voltage control. There is hindrance in the vein of higher levels because of using more number of semiconductor switches. It may lead to huge size and increases the cost of the inverter. So the proposed method is well suited for a high power application and it is built with one DC source and six semiconductor switches. This paper is a simple and flexible technique to reduce common-mode voltage for a seven level hybrid cascaded inverter. The MCHBMLI is established based on five levels H-bridge cascaded inverter. This method also reduces the switching losses and is simple to be implemented in a common processor. This topology has only one dc source, and diverse voltage levels are generated by using this voltage source along with floating capacitors charged to voltage levels. Total Harmonic Distortion obtained from the above HPWM techniques. The Seven level MCHBMLI circuit is simulated and verified by using MATLAB/Simulink.**

**Index Terms— Multilevel inverter (MLI), Modified Cascaded H Bridge Multilevel inverter (MCHMLI), Total harmonic distortion (THD), Cascaded H-bridge(CHB), Neutral point clamped (NPC),In-phase disposition(IPD), Alternative phase opposite disposition(APOD) and Carrier based PWM (CPWM).**

## I. INTRODUCTION

Multilevel inverter has emerged recently in the area of high power medium voltage applications due to their advantages such as output waveform improvement which reduces the harmonic content which in turn reduces the size and cost of the filter and the level of electromagnetic interference (EMI) generated by switching operation[1]. Low harmonic distortion waveforms are generated, at relatively low switching frequencies, Also, many of the trouble encountered in two-level inverters such as high dv/dt, high electromagnetic interference, higher voltage stress on the devices, elevated switching losses, The multilevel inverters are classified as the three topologies are prominent. They are the neutral point- clamped (NPC) inverter [2], the flying capacitor (FC) inverter [3], and the cascaded H-bridge (CHB) inverter [4]. The main drawback in Conventional cascaded is that when levels are increasing it requires more number of semiconductor switches apart from the aforesaid topologies, a number of new topologies, including many hybrid multilevel configurations have been proposed [5],[6].

The cascaded H-bridge multi-level inverter is the most suitable topology. Medium-voltage High-power motor drives fed from multilevel inverters are being increasingly used in the industry for various applications. The level of extension is easy.

- No voltage unbalancing problem
- It has modular structure

## II. PROPOSED HYBRID CASCADED 7 LEVEL INVERTER

The proposed seven level inverter consists of a hybrid cell with a separate DC source [7]. The Hybrid cell has a full bridge inverter which has four sequential switching MOSFET devices with additional two switches to get 7 level output voltages. The exclusive arrangement of multilevel voltage source inverters allow them to achieve high voltages with reduced harmonics without including the utilization of transformers or series connected synchronized switching devices. The main advantages of cascaded H-bridge inverter are that it requires least number of components and soft switching are used. The habitual cascaded seven level inverter require twelve switches and three dc sources separately. The main drawback in conventional cascaded multi level inverter is the increase in number of semiconductor switches with increase in level of the output. The proposed topology is designed with single



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dc source and six switches and also it consists of some additional features like minimum number of switches conducting at a specific interval of time. Additionally hybrid PWM methods are introduced to reduce the harmonics.

This is a comparative study of different topologies of MLI for producing the same seven-level output. The output voltage of the MCHMLI have seven voltages levels (0, $V_{dc}/3$,$V_{dc}/2$,$V_{dc}$,-$V_{dc}/3$,-$V_{dc}/2$, and -$V_{dc}$). The features are

- Reduced number of switches.
- Higher speed capability
- Low output switching frequency
- Low switching loss
- High conversion efficiency

The indiscriminate expression for the number of switches and the number of dc sources for the proposed topology is given by:

S = (N+5)/2

Where N= number of levels and S= number of switches.

V = (N-1)/2

Where V=number of dc voltage sources.

The method is to either eliminate or reduce the CMVs at the source itself by modifying the PWM converter topology and the modulation schemes. A number of such schemes have been reported in the literature.

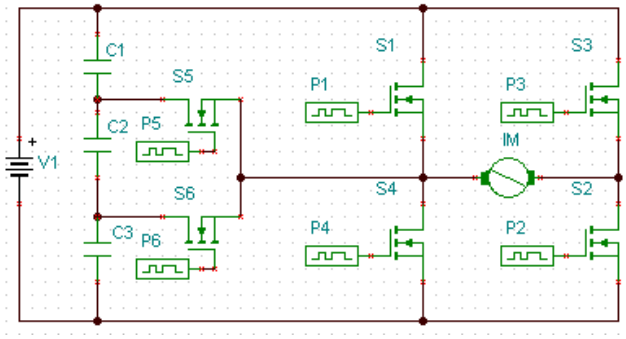


Figure 2.1: Seven level Hybrid Cascaded H Bridge Multi level inverter (HCBMLI)

Figure 2.1 shows the circuit arrangement of proposed topology which consists of six switches and a single DC source is used. Switch S5 and S6 are used for reverse polarity and the remaining switches are used to generate the levels in both positive and negative sides to produce the desired five level waveforms.

A. Modes of operation.

The Proposed Multi level inverter has the following modes of operation. They are

Mode I

In this mode the current flows through $C_3$-$C_2$-$C_1$-S1-load-$S_2$. The output voltage level is $V_{DC}$. The picturesque representation of this mode of operation with current direction is shown in this figure.2.2

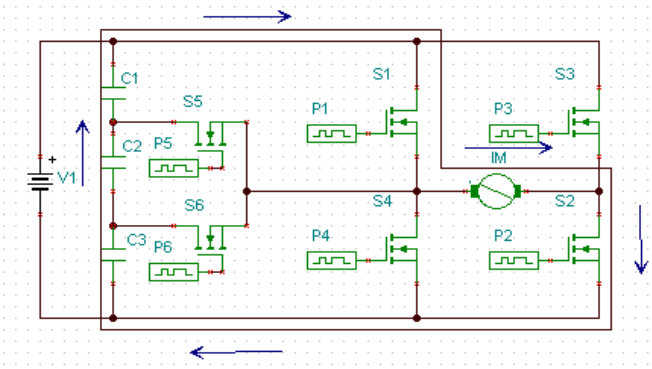


**Figure 2.2** Mode 1 operation of MCHB inverter

Mode II

In this mode the current flows through $C_3$-$C_2$-S5-load-$S_2$ the level of output voltage in this mode is 2VDC/3. The picturesque representation of this mode of operation with current direction is shown in figure 2.3.

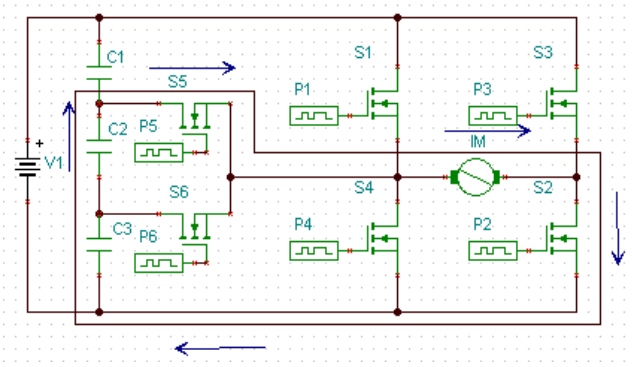


**Figure 2.3** Mode II operation of MCHB Inverter

Mode III

In this mode the current flows through $C_3$—S6-load-$S_2$The level of output voltage in this mode is VDC/3 The picturesque representation of this mode of operation with current direction is shown in figure.2.4.



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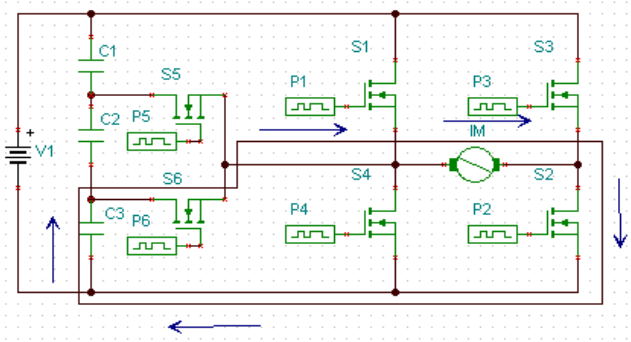


**Figure 2.4** Mode III operation of MCHB Inverter.

MODE IV

In this mode the current flows through $C_1$-$S_5$-load$S_3$

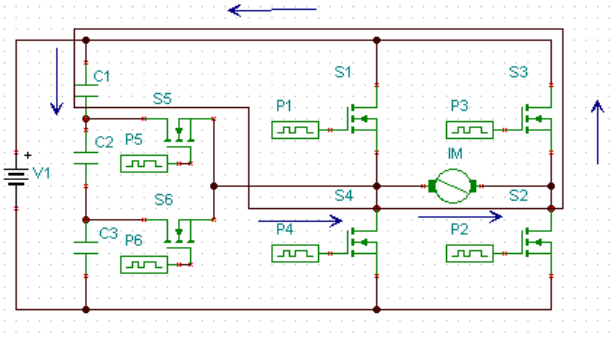


**Figure 2.5** Mode IV operation of MCHB Inverter

The level of output voltage in this mode is –Vdc/3. The picturesque representation of this mode of operation with current direction is shown in figure.2.5.

Mode V

In this mode the current flows through $C_1$-$C_2$-$S_6$-load-$S_3$. The level of output voltage in this mode is -2Vdc/3. The picturesque representation of this mode of operation with current direction is shown in figure.2.6.

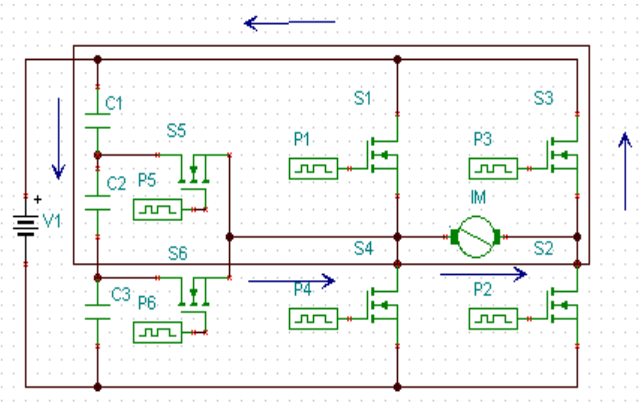


**Figure 2.6** Mode V operation of MCHB Inverter

Mode VI

In this mode the current flows through $C_1$-$C_2$-$C_3$-$S_4$-load-$S_3$. The level of output voltage in this mode is -Vdc. The picturesque representation of this mode of operation with current direction is shown in figure.2.7.

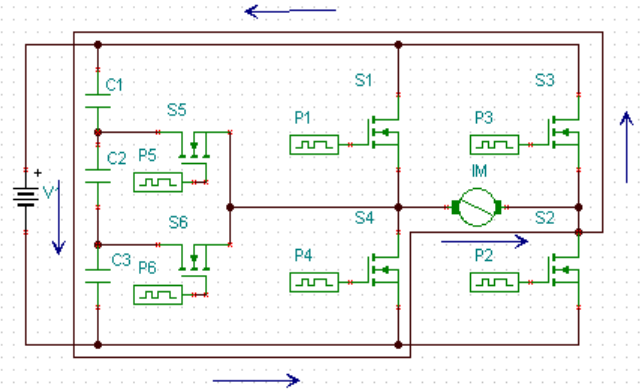


**Figure 2.7** Mode V operation of MCHB Inverter

Proper sequential switching of inverter produces five level output voltages (0, Vdc/3,Vdc/2,Vdc,-Vdc/3,-Vdc/2, and -Vdc.). A sequential switching state of the proposed hybrid inverter is given in the Table 2.1.

Table 2.1: Switching state of inverter

| S.No. | S1 | S2 | S3 | S4 | S5 | S6 | OUTPUT VOLTAGE |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | VDC |
| 2 | 0 | 1 | 0 | 0 | 1 | 0 | 2VDC/3 |
| 3 | 0 | 1 | 0 | 0 | 0 | 1 | VDC/3 |



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| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 4 | 0 | 0 | 1 | 0 | 1 | 0 | -VDC/3 |
| 5 | 0 | 0 | 1 | 0 | 0 | 1 | -2VDC/3 |
| 6 | 0 | 0 | 1 | 1 | 0 | 0 | -VDC |

III>HYBRID MODULATION STRATEGY

A single reference signal is compared with six carrier signals to generate HPWM signal. A novel modulation technique [4-6] was proposed to generate HPWM signals. The carrier signals have the same frequency with different amplitude. To generate the switching pattern the carrier signals were compared with the reference signal. The carrier signal Vcarriers would be compared with Vref until Vref reaches zero. The required switching patternare generated as mentioned in the Table2.1.

The analysis is only for one-phase, but two other phases are similar. The three-phase circuit diagram of a hybrid seven-level cascade inverter is illustrated in Figure 2. The switches take on the value "1" when switches are closed and the value "0" when opened. In order to avoid shoot-through fault, switches S1x and switches S4x (x= 1, 2) are never closed at the same time. It is the same with switches S3x and S2x. The output phase voltage of single-phase circuit is the sum of each H-bridge output voltages. The relation of this voltage and the switching states is shown in Table 2.I.

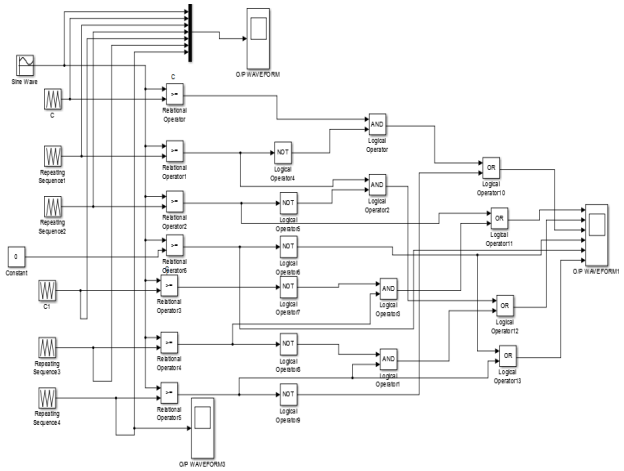

**Figure 3.1:** Hybrid PWM pulse generation Scheme.

## IV. SIMULATION RESULTS

Cascaded SEVEN level inverter operation and its results are studied WITH IM load. The simulation diagram of Hybrid Cascaded H bridge multi level inverter is shown in figure 41.

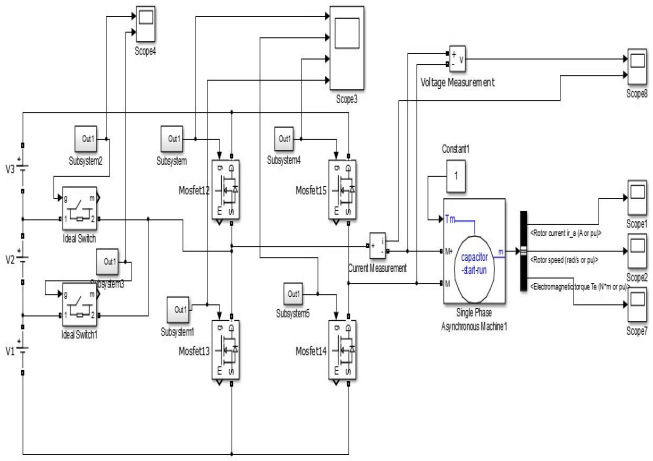

**Figure 4.1:** Simulation diagram for Hybrid Cascaded H Bridge Inverter**.**

The simulation diagram of the proposed inverter is shown in Figure 4.1 All the switches used in this circuit are MOSFET. The switch $S_5$ and $S_6$ are bidirectional and the remaining switches are unidirectional and load is taken as induction motor .The dc source voltage is taken as 150V. The circuit used for generating the pulses is shown in Figure 3.1. The circuit is designed in Matlab/simulink and the generation of pulses have been made by comparing every carrier wave with the sine wave and the resultant pulses are given to the appropriate switches to produce the seven level staircase waveform.

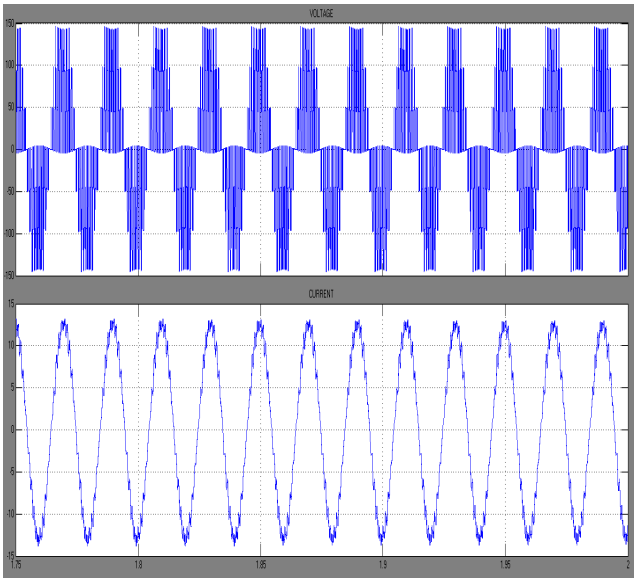


**Figure 4.2:** Output Voltage and Current waveform for HCBMLI



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The waveforms of the output voltage and the output current are shown in Figure 4.2. Here the switch $S_1$ & $S_2$ has been given with the pulses of $+V_{dc}$, whereas $S_3$ & $S_4$ has been given with the pulses of $-V_{dc}$. The total harmonic distortion of HPWM scheme is viewed through the FFT window and is shown belo

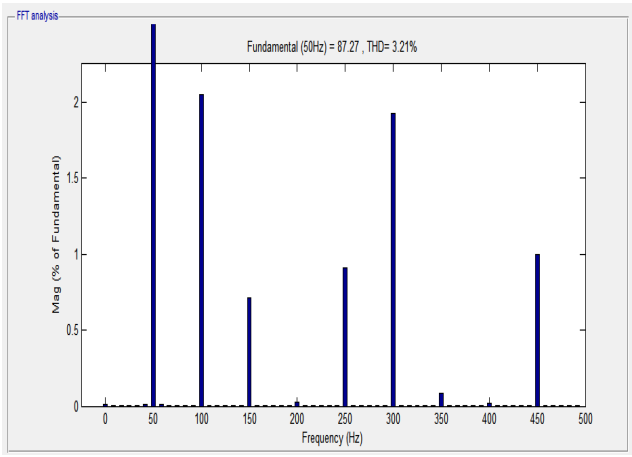


**Figure4.3:** Fast Fourier Transform(FFT)analysis for HCBMLI Fast Fourier Transform (FFT) analysis of HCBMLI is show in figure 4.3. Total harmonic istortion is 3.21% with a fundamental frequency of 50 Hz for its output voltage. The proposed topology is better when compared to the existing topologies.

## V. CONCLUSION

A Novel HPWM Scheme with reduction of switches for 7 level inverter has been presented in this paper. The proposed method requires only single DC sources. The novel PWM technology for harmonic reduction is simulated using MATLAB/SIMULINK. The performance of the Multi level inverter has been analysed using FFT analysis. By mounting the number of steps, waveform approaches the required sinusoidal shape and THD is reduced. The proposed modulation strategy of the multilevel inverter with fuel cell in place of dc sources has a greater scope in applications involving electrical vehicles.

A new hybrid seven-level inverter topology with elimination of CMVs has been presented in this paper. This is of great significance to high-power drives fed from PWM inverters, in which one of the major reasons for mechanical failure is attributed to the damage caused to the bearings due to the common-mode leakage currents.

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