Multi Carrier PWM and Selective Harmonic Elimination Technique For Cascade MultilevelInverter

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Multi Carrier PWM and Selective Harmonic Elimination technique for Cascade Multilevel Inverter

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***Abstract* —This paper presents the multi carrier pulse width modulation (MCPWM) and selective harmonic elimination (SHE) technique for cascade multilevel inverter (CMI) to reduce the total harmonic distortion (THD) of the output voltage waveform. A comparison has been done between the SHE and MCPWM technique to show the advantage of SHE technique over the MCPWM technique. To find the accuracy of total harmonic distortion (THD) between the MCPWM and SHE technique is achieved by comparing the FFT based result for nine level cascade multilevel inverter.**

Index Terms—Cascade multilevel inverter, Multi carrier pulse width modulation, Selective harmonic elimination technique, Total harmonic distortion.

I. INTRODUCTION

MULTILEVEL inverters are one of the extensively studied research area of power converters. The multilevel inverter is used to produce sinusoidal voltage waveform from several levels of dc voltage. However, two-level voltage source converter incapable to get good system performance and efficiency such as optimum filter size, THD and losses. The improved performance and efficiency of high voltage system can be achieved by the use of multilevel inverter [1]. With increased number of levels in cascade multilevel inverter, the output voltage quality increases in terms of total harmonic distortion. Since, the number of levels increases, the intricacy of control schemes and voltage imbalance condition occurs.

Among the three commercial topologies of multilevel voltage source inverter such as : neutral point clamped, cascade multilevel inverter and, flying capacitor, use of CMI results in higher output voltage and power levels and are more reliable due to its modular topology [2].

The levels in a CMI are formalized as k = 2s + 1, where k defines the output phase voltage level and *s* defines the number of dc sources used in single phase. The use of multilevel inverters has a great enthuse to reduce of voltage stress on the switching devices [3], less harmonic distortion, producing of smaller common mode voltage, less electromagnetic compatibility problems and capable to produce higher voltage with reduced device rating.

The CMI is a good solution due to its modularity and simplicity in control mechanism. Fig.1 shows the basic structure of CMI, in which four cells are connected in series to get nine level of output voltage per phase.

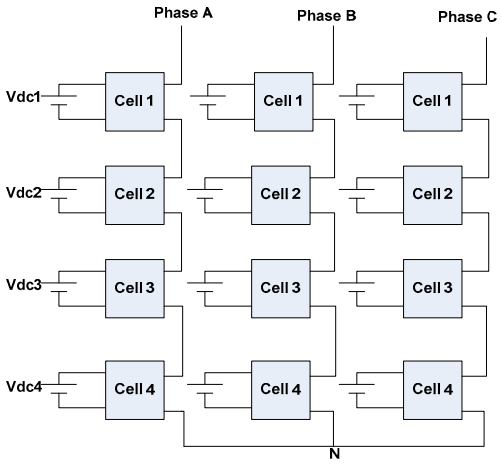

Fig.1 Three-phase nine-level CMI

II. CASCADE MULTILEVEL INVERTER TOPOLOGIES

There are various CMI configuration available for both single-phase and three-phase application as shown in fig.2. The single phase cascade half bridge is a one leg converter consisting of two switching element is used to produce two level output of the voltage source converter. The cascade H bridge inverter uses string of single phase full bridge inverter connected in series to construct multiple phase leg [4]. Cascade H bridge topology allows a low voltage rating of the semiconductor devices. The operating voltage and manufacturing cost plays a important role to decide number of power cells in cascade H bridge invverter. For instance, a nine-level inverter will use low rating

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device compared two level inverter for MV drives. Cascade H bridge inverter requires separate dc source for one phase leg of equal dc sources which are capable to produce output voltage level in proportional to number of cells used in CMI. With use of unequal dc sources number of levels are incresed in CMI and this topology is known as CMI with unsymmetrical dc sources [3].

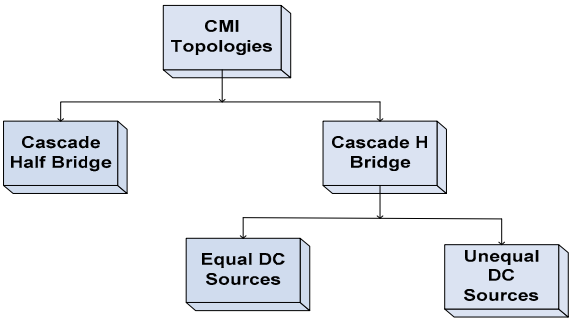

Fig.2 CMI Topologies

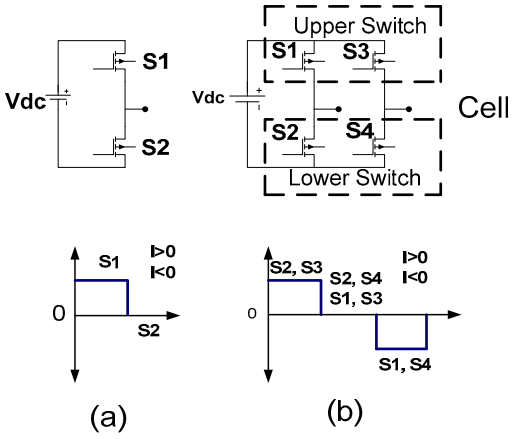

Fig.3 Single-phase CMI (half bridge) inverter (a), Single-phase CMI (full bridge) inverter (b)

III. MODULATION TECHNIQUES

The modulation technique used for multilevel inverters can be classified according to the switching frequency [5], as shown in fig.4. In the fundamental switching frequency approach, the switching losses are less, lower order harmonics are present in the output voltage waveform whereas, in the PWM method, due to higher switching frequency, switching losses are more and higher frequency harmonics are present at output voltage waveform [6]. The harmonic performance of SHE-PWM is relatively good for low level numbers as compared to the space vector and phase shifted MCPWM. However, the number of level increases the performance of phase-shift carrier base modulation increases more rapidly than SHE technique [7]. In multilevel converters, the switching state redundancy is a common phenomenon which provides a great flexibility for switching pattern design, especially for space vector modulation schemes.

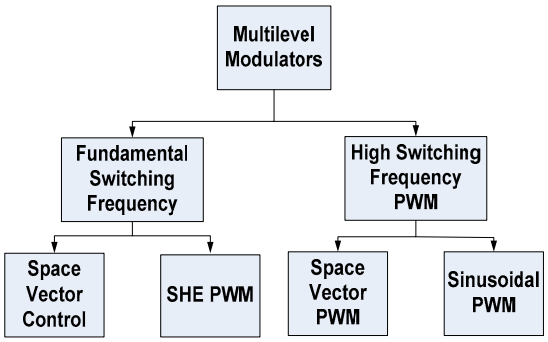

Fig.4 Classification of modulation techiques for multilevel inverter

A) Multi Carrier PWM

Multi carrier based PWM techique is used to regulate the output voltage and to reduce total harmonic distortion. In multi carrier PWM method, single sinousoidal is compared with each carries to determined the switched output voltage for the converters [8].
Generally, two modulation techiques are used for multilevel inverter such as phase shifted MCPWM and level shifted MCPWM [9].

1) Phase shifted multi carrier PWM

Phase-shift MCPWM is the most common strategy for the cascade multilevel inverter, with an improved harmonic performance being achieved when each single phase inverter is controlled using three-level modulation [9]. To get higher ripple frequency than switching frequency, the phase-shifted PWM can be used for the multilevel inverter [10]. Here each carrier is linked to an individual cell and by having a suitable phase shift among carriers multilevel stepped waveform is achieved. As switching device in each cell have same switching frequency conditions therefore rotation of switching pulses is not required.
In this technique, all the triangular carriers have the same frequency and the same peak-to-peak amplitude [11], but the phase shift occurs between any two adjacent carrier waves, given by $\Phi_{cr} = \frac{360}{k-1}$ where k is the number of levels of output voltage. In this paper, eight carrier waves are used with 45^0 phase shift between any two adjacent carrier waves for nine-level CMI and the phase voltage of single phase nine-level inverter is determined by: $V_{AN} = V_{cell\ 1}+V_{cell\ 2}+V_{cell\ 3}+V_{cell\ 4}$.

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Where $V_{cell\ 1}$, $V_{cell\ 2}$, $V_{cell\ 3}$ and $V_{cell\ 4}$ represents the output voltage of cell 1, cell 2, cell 3 and cell 4 respectively.
The simplified phase shifted modulation schematic is shown in fig.5 in which upper switches S1 and S3 of cell as shown in fig.3 (b) are triggered by two carrier waves having a phase shift of 180^0 to each other while lower switches of cell are triggered in complementary manner with respect to their corresponding upper switches.

2) Level shifted multi carrier PWM

In this scheme, k-1 carriers (triangular) are used for k level CMI, each carrier has same amplitude and frequency. which have same frequency and amplitude [8]. Here each voltage level is associated with a carrier. When a particular voltage level is to be generated, reference wave should be higher than that particular carrier. This scheme will have unequal switching condition for device in each cell, leads to unequal power distribution among cells hence rotation of pulses among power cells can not be avoided. It can be further divided into three types, in phase disposition (IPD), where all the carriers are in phase; alternative phase opposite disposition (APOD), where all carriers are alternatively in opposite disposition and phase opposite disposition (POD), where all the carriers above the zero reference are in phase but in opposition with those below the zero reference. The simplified level shifted modulation schematic is shown in fig.6 in which gating signal for upper switches S1 and S3 of cell of fig.3 (b) is provided by two carrier waves, one is above the zero reference and another is below the zero reference while lower switches of cell are triggered in complementary manner with respect to their corresponding upper switches.

B) Selective Harmonic Elimination Technique

In high-power application, the maximum switching frequency is limited due to thermal losses [12], [13]. SHE is an efficient method to obtain output signals with lower harmonic content then other modulation technique. Selective harmonic elimination pulse-width modulation (SHE-PWM) provides an acceptable level of performance used for high-power medium-voltage cascaded multilevel inverter with both equal and unequal dc sources used in constant frequency utility applications. SHE-PWM is based on the Fourier series decomposition of the periodic PWM voltage waveform generated by the power electronics converter, as given in equation (1) [14] .By the use of Selective harmonic elimination technique, selected harmonics are eliminated with the smallest number of switching. SHE technique is used to optimize switching angles of a cascaded multilevel inverter so as to produce required fundamental voltage along with improved staircase waveform in terms of total harmonic distortion. Number of non-linear transcendental equation will be s and number of harmonics to be eliminated becomes (s-1) in SHE formulation if the number of cells used in cascade multilevel inverter is s per phase.
For the nine-level CMI, 5^{th}, 7^{th} and 11^{th} harmonics needs to be eliminated with the equation (2) formulation having the advantage of quarter wave symmetry and further reduction in THD takes place because inverter line to line voltage does not contain any triplen harmonics.

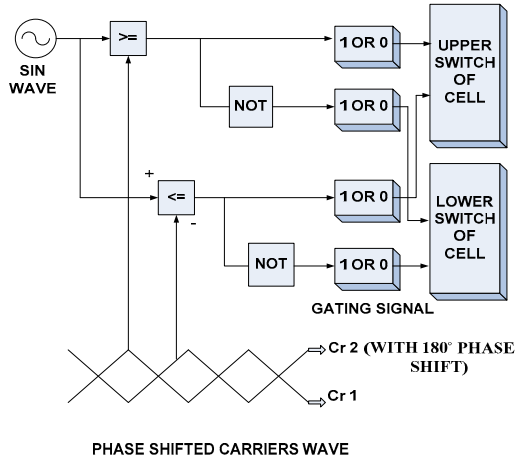

Fig.5 Simplified phase shifted modulation schematic

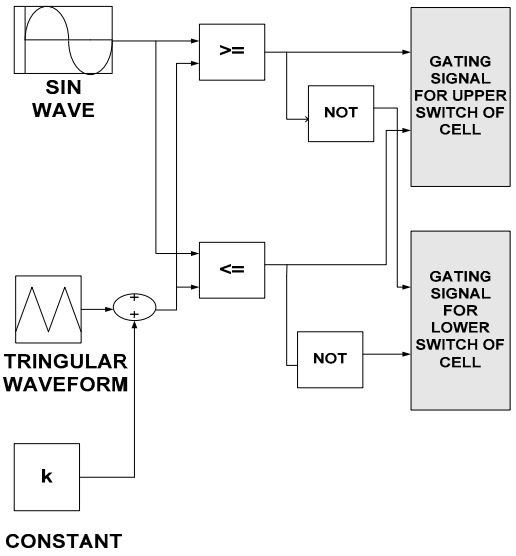

Fig.6 Simplified level shifted modulation schematic

$$f_N(t) = \frac{a_0}{2} + \sum_{n=1}^{N}\left(a_n \cos\left(\frac{2\pi nt}{T}\right) + b_n \sin\left(\frac{2\pi nt}{T}\right)\right) \quad (1)$$

$$\cos(5\alpha_1)+\cos(5\alpha_2)+.\cos(5\alpha_3)+\cos(5\alpha_4) = 0$$
$$\cos(7\alpha_1)+\cos(7\alpha_2)+\cos(7\alpha_3)+\cos(7\alpha_4) = 0 \quad (2)$$

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$\cos(11\alpha_1)+\cos(11\alpha_2)+\cos(11\alpha_3)+\cos(11\alpha_4) = 0$

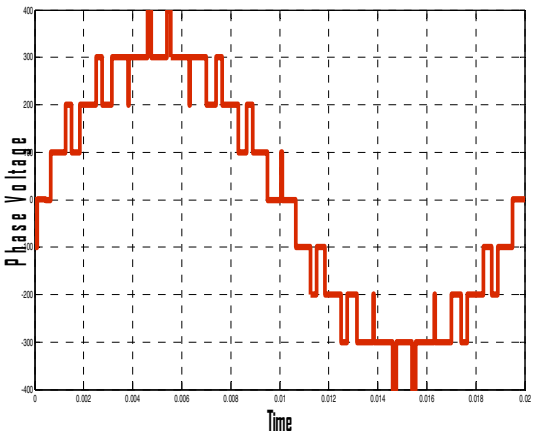
Comparison among the different modulation technique has been done on the basis of semiconductor device conduction period, switching frequency, and rotating of switching patterns and line to line voltage THD as shown in table.1.

TABLE I
COMPARISON AMONG PHASE SHIFTED, LEVEL SHIFTED AND SHE MODULATION

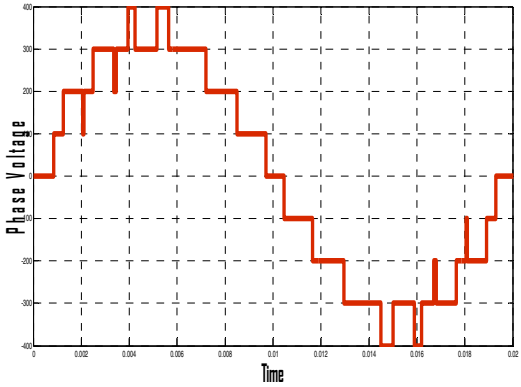
Comparison	Phase shifted modulation	Level shifted modulation	SHE modulation
Device conduction period	Same for all device	different	Same for all device
Device switching frequency	Same for all device	different	Same for all device
Rotating of switching patterns	Not required	required	Not required
Line to Line Voltage THD	good	Very good	Better

IV. SIMULATION RESULT

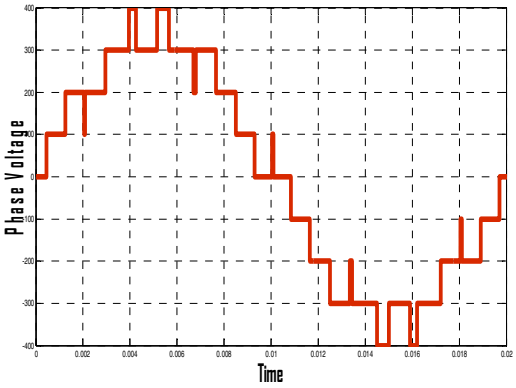
Fig.7 shows the simulated phase voltage waveform for a nine-level cascade multilevel inverter using the multi carrier PWM and SHE technique. The inverter operates at 50 Hz frequency. Table.2 shows the voltage THD for different modulation methods. Compared with the phase shifted and level shifted modulation, THD of the SHE method is much improved. The THD is also improved in the case of three phase line to line voltage as comparison to single-phase for all modulation strategy. In-phase deposition level shifted modulation strategy provides the best line to line voltage THD profile among other level shifted and phase shifted multi carrier pulse width modulation technique.



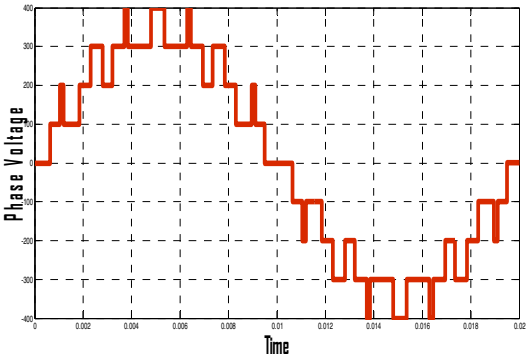
(a) phase shited modulated single-phase voltage waveform



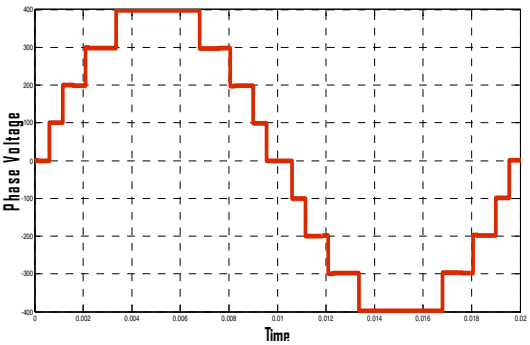
(b) level shited (POD) modulated single-phase voltage waveform



(c) level shited (APOD) modulated single-phase voltage waveform



(d) level shited (IPD) modulated single-phase voltage waveform



(e) SHE modulated single-phase voltage waveform

Fig.7 Modulated voltage waveform

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TABLE.II
VOLTAGE THD FOR DIFFERENT MODULATION METHODS

Modulation Techniques	Voltage THD	
phase	1-Φ	3-Φ
Phase shifted modulation	17.62%	14.82%
LS (POD) modulation	16.22%	14.98%
LS (APOD) modulation	16.35%	12.72%
LS (IPD) modulation	19.67%	11.12%
SHE modulation	9.60%	6.89%

V. CONCLUSION

A nine-level cascade multilevel inverter is presented in this paper. Multi carrier PWM and SHE modulation method are employed for nine-level CMI. The principle of the MCPWM and SHE has been verified by simulation result. In order to analyze the THD performence of phase voltage and line voltage among the various modulation technique, comparison has been done. The accuracy of SHE techinque over the other modulation technique is verfied by the simulation result.

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