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Pipeline and Parallel Processor Architecture for Fast Computation of 3D-DWT using Modified Lifting Scheme

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Abstract— A pipelined parallel processing 3D DWT architecture is designed in this paper based on lifting scheme algorithm with 9/7 wavelet filters. The 3D DWT architecture process a 512x512 image with 8 groups of frames sequentially with improved throughput. The first stage computes 1D-DWT along the rows with 4 parallel processors, the memory interface with FIFO reduces latency between first stage and second stage that computes 2D DWT computation.3D DWT computes wavelet coefficients in the temporal direction and designed to operate from 512*4 clock cycles in sequence along with 1D and 2D DWT computation. The FIFO designed synchronizes the data movement. Memories at every stage are designed to store the parallel processed data. The proposed architecture has high performance and is suitable for high speed, low power and portable applications. With utilization of 51% of slice registers 3D-DWT architecture implemented on Virtex-5 FPGA and frequency of operation is 373 MHz. The designed DWT-IDWT can be used as IP Core.

Index Terms: Lifting scheme, pipelined architecture 3D DWT, parallel processing, FPGAs.

I. INTRODUCTION

DWT(Discrete Wavelet Transform) mostly used for image coding [1] since the signals are decomposed into sub-bands with frequency and time information and attains a high compression ratio [2]. Features of DWT are progressive image transmission (by quality, by resolution), ease of compressed image manipulation, region of interest coding, etc. The JPEG 2000 integrates the DWT into its standard [3].

In recent times, some VLSI architectures have been projected to realize single chip designs for DWT [4]. Usually, such algorithms implemented using programmable DSP chips or application specific integrated circuits (ASICs). To perform the convolution, fast multiplier is critical in making the operations efficient.

Anirban Das, et al [5] proposed lifting based running 3-D DWT architecture, a powerful image and video compression algorithm. Modified lifting scheme with optimized architecture implemented on FPGA, the architecture does not address pipelined architecture and hence reduces throughput. An efficient VLSI architecture was proposed[6] by Chin-Fa Hsieh, et al for the implementation of 1-D lifting-based DWT. Both folded (higher hardware utilization) and the pipelined (speeds up clock rate) schemes are applied in the proposed architecture. Later, efficient VLSI architecture for 2-D lifting-based 5/3 filter DWT was reported in [7].But high speed & less area is attained by using systolic array as reported in [11], the 3D DWT architecture proposed is implemented using DWT [13]. The architecture is based on the pipelined and folding scheme processing to achieve near 100% hardware utilization and reduce the silicon area. The proposed efficient 2-D lifting-based DWT VLSI architecture uses lossless 5/3 filter and pipelined processing. The architecture may have almost 100% hardware utilization.

The advantages of the proposed DWT are higher hardware utilization, less memory requirement, and regular data flow. The architectures discussed above are suitable for FPGA implementation. In this work, lifting equations consisting of predict and update stages are designed using micro core engines that compute intermediate lifting output that are pipelined to improve throughput. The micro core engines are designed to process the data in all three dimensions leading to 3D DWT architecture. The proposed architecture achieves high throughput and reduces latency. Section II presents 3D DWT architecture with pipelined architecture, five stages pipelined with four fully parallel architecture. Section III discusses the proposed pipelined architecture for 3D DWT architecture. The results are presented in section IV followed by Conclusion in section V.

II. 3D-DWT Architecture

3D encoding of video [1, 2, 3, 4, 5] provides higher compression and image quality compared to MPEG [6, 7, 8, 9] based compression techniques. DWT transforms input imageinto sub bands and encoded using appropriate encoding techniques leading to compression. 3D encoding of input data reduces memory requirements with data processing in the temporal discrete wavelet transform (DWT) on 3D blocks coming from a temporal splitting of the sequence. 3D wavelet transforms performs 2D DWT on each frame and an additional 1D DWT in the time direction [16] as shown in Figure 1. The 3D architecture performs 2D DWT on every frame, with each frame decomposed to four sub bands. Each sub band is grouped into LL, LH, HL and HH bands and 1D DWT is performed in the temporal domain and hence eight sub bands of LLL, LLH, LHL,

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LHH, HLL, HLH, HHL and HHH are obtained.Input data consisting N x N x M (N represents number of pixels, M represents number of frames) is grouped into N x N x 8 group of frames for data processing. Every GOP consists of 8 frames each of size N x N is first processed using 2D DWT. Each 2D DWT consists of two stages of row processing and column processing. Row processing and column processing blocks consists of high pass and low pass filters that decomposes the 1D data into high pass and low pass DWT filter coefficients. The row processing consists of one stage of high pass and low pass filters that decomposes the row elements into L and H sub bands. The column processing block consists of two parallel stages of high pass and low pass filters that process the L and H sub band of data to further decompose the data into LL(low pass), LH and HL and HH (high pass) sub bands.

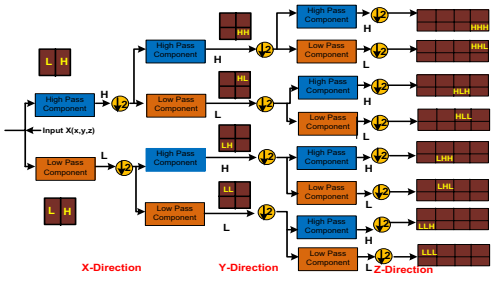

Fig 1. 3D DWT Processing

The 1D-DWT process the input samples in rows, every row consisting of N pixels is processed and down sampled to obtain N/2 wavelet coefficients that are stored in a separate memory. The processing of N rows consisting of N pixels consumes 9*N2 multiplication and 9*N2-1 additions.

G0 = HighPass Filter.

H0 = LowPass Filter.

↓ = Down Sample by 2

Lifting based DWT computation is mostly being used for DWT computation. Lifting scheme reduces the number of arithmetic operations, memory elements and computation time. The block diagram for lifting scheme [6] is shown in Figure 2.

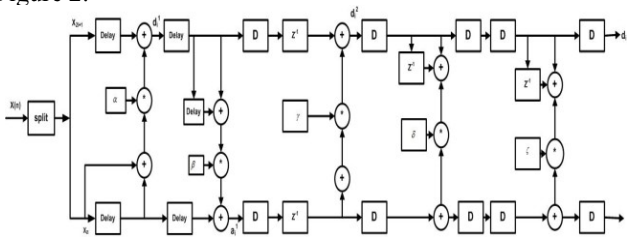

Fig 2. Lifting Scheme Architecture

The 9/7 filter coefficients are reduced to α, β, γ, δ, and ζ lifting coefficients. The input signal x(n) or (x_i) splits into even part x_{2i} and odd part x_{2i+1}. Subsequently, the first step of lifting is performed given by,

$$d_i^1 = \alpha\left(x_{2i} + x_{2i+2}\right) + x_{2i+1} \quad (1)$$

$$a_i^1 = \beta\left(d_i^1 + d_{i-1}^1\right) + x_{2i} \quad (2)$$

The first equation is predictor P1 and the second equation is updater U1. Then the second lifting step is performed resulting in equations (3) and (4):

$$d_i^2 = \gamma\left(a_i^1 + a_{i+1}^1\right) + d_i^1 \quad (3)$$

$$a_i^2 = \delta\left(d_i^2 + d_{i-1}^2\right) + a_i^1 \quad (4)$$

The third equation is predictor P2 and the fourth equation is updater U2. Thereafter, the scaling is performed in order to obtain the approximation and detail coefficients of DWT as given in equations (5) and (6).

$$a_i = \zeta a_i^2 = G_1 \quad (5)$$

$$d_i = d_i^2 / \zeta = G_2 \quad (6)$$

The equations (5) and (6) are correspondingly scales G_1 and G_2. The predicted step helps to determine the correlation between the sets of data and predicts even data samples from odd. These samples are used for updating the present phase. It may be observed that the computation of the final coefficients requires 6 steps. Each stage of computation consists of a_i and d_i coefficients that require three samples of data which requires three clock cycles. The a_i data depends upon d_i and d_i computation requires x_i. These interdependency of data increases delay and reduces throughput, in order to reduce computation time and improve throughput a novel architecture is proposed in this work that is made up of multiple processing engines that independently compute the a_i and d_i coefficients with time delay.

A. Five stage pipelined with four fully parallel architecture

The lifting equations presented in Equation (1) to (6) are computed for various time intervals and are shown in Table 1.For i=0 to i=3 the lifting equations are computed, the predict and update computation requires three samples as inputs. Table 2 presents the delay in predict and update coefficient computation. The first approximation and detail coefficient is computed at the end of 4th clock cycle. The throughput is found to be two clock cycles. In order to improve the throughput to one clock cycle, a modified architecture is proposed. The proposed architecture delays the computation of update1, predict 2 and update 2 computations even after them being generated. As the delay in predict 1 sample is two clock cycles, and so update 1, computation of update 1 starts after 12 clock cycles.

At the end of 12 clock cycles there are 6 predict 1 sample generated and stored in memory. Thus computation of update 1 clock cycle is forced delayed by 12 clock cycles, and from 13th clock cycle update 1 is computed. Further the computation of predict 1 is delayed by 12 clock cycles as compared with update 1. Thus the first predict coefficient 1 is obtained at the end of 25th clock cycle.

Similarly, computation of update 2 is delayed by another 12 clock cycle. Introducing 12 clock cycle delay between

intermediate steps ensures that minimum of six samples of data are available in the memory from the previous stages. The proposed architecture reads the row elements from the main memory into the intermediate memory1. The control unit is designed to read 4N elements into the intermediate memory1. The 4N elements are then processed by the first micro core engine to compute the d^1_i output samples that are stored in intermediate memory2. For the first 12 clock cycles three micro core engines are disabled.

After 12 clock cycles the second micro core engine is enabled to process data from intermediate memory 2 and the first core processes data from memory1. Further the third and fourth micro core engines are enabled after 36^{th} and 48^{th} clock cycle. The first micro core engine completes the data processing of all rows in N*N clock cycles. The total delay in computing the 1D DWT is (N*N + 48) clock cycles. As the proposed architecture introduces forced delay in computation of predict and update stages, the throughput is reduced to 1 clock cycle. Table 3 shows the computation delay and the throughput in the proposed architecture. The micro core engines are designed to compute predict and update phases with parallel processing approach. The intermediate memory that stores the input data is designed to be a PIPO register that is designed to access all the contents in parallel.

The input samples are accumulated and multiplied as in lifting equations discussed. In every clock cycle four predict1 samples are generated and are demultiplexed into appropriate locations in intermediate memory 2. The d1i output samples generated are stored in intermediate memory, at the beginning of 13th clock cycle the samples are read into another PIPO register. The micro core engine is enable at the 13th clock cycle and the PIPO data is read into the parallel processing units. For computation of update 1, it is also required to have the input samples, hence there are two PIPO registers one for d_i samples and one for input samples.

The computed a1i are stored in intermediate memory2. Similarly the predict2 and update2 micro engines are designed to process data in parallel with intermediate registers and PIPO registers. The main clock is used to read data from input memory to four intermediate memories. The processed data out from the four parallel processing unit needs to be reorganized for which a demultiplexer unit is designed. The di computation unit consists of four parallel processing modules. FSM based control unit is designed to control the main memory, intermediate memory, di computation unit, demultiplexer and the output memory. The control signals from the FSM are synchronized with regard to main clock and hence data loss is prevented. Figure 5 shows the di computation unit that consists of an internal FSM to enable the memory unit and the arithmetic processing elements. The FSM control unit controls the data synchronization between data movement from registers to the final output computation.

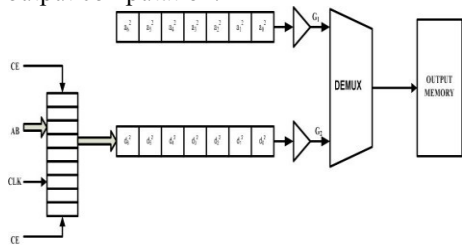

Fig 3. Micro core engine for final stage of lifting computation

TABLE I Lifting equation iterations

	Predict 1	Predict 2	Update 1	Update 2	Samples
i	$d_i^1 = \alpha\left(X_{2i} + X_{2i+2}\right) + X_{2i+1}$	$d_i^2 = \gamma\left(a_i^1 + a_{i+1}^1\right) + d_i^1$	$a_i^1 = \beta\left(d_i^1 + d_{i-1}^1\right) + Z_{2i}$	$a_i^2 = \delta\left(d_i^2 + d_{i-1}^2\right) + a_i^1$	
0	$d_0^1 = \alpha\left(X_0 + X_2\right) + X_1$	$d_0^2 = \gamma\left(a_0^1 + a_1^1\right) + d_0^1$	$a_0^1 = \beta\left(d_0^1 + d_{-1}^1\right) + X_0$	$a_0^2 = \delta\left(d_0^2 + d_{-1}^2\right) + a_0^1$	3
1	$d_1^1 = \alpha\left(X_2 + X_4\right) + X_3$	$d_1^2 = \gamma\left(a_1^1 + a_2^1\right) + d_1^1$	$a_1^1 = \beta\left(d_1^1 + d_0^1\right) + X_2$	$a_1^2 = \delta\left(d_1^2 + d_0^2\right) + a_1^1$	3
2	$d_2^1 = \alpha\left(X_4 + X_6\right) + X_5$	$d_2^2 = \gamma\left(a_2^1 + a_3^1\right) + d_2^1$	$a_2^1 = \beta\left(d_2^1 + d_1^1\right) + X_4$	$a_2^2 = \delta\left(d_2^2 + d_1^2\right) + a_2^1$	3
3	$d_3^1 = \alpha\left(X_6 + X_8\right) + X_7$	$d_3^2 = \gamma\left(a_3^1 + a_4^1\right) + d_3^1$	$a_3^1 = \beta\left(d_3^1 + d_2^1\right) + X_6$	$a_3^2 = \delta\left(d_3^2 + d_2^2\right) + a_3^1$	3

TABLE II Throughput and computation delay in generic lifting architecture

Clock	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Input	x_1	x_2														
Predict1			d^1_0	d^1_1		d^1_2		d^1_3		d^1_4		d^1_5		d^1_6		d^1_7
Update1			a^1_0	a^1_1		a^1_2		a^1_3		a^1_4		a^1_5		a^1_6		a^1_7
Predict2				d^2_0		d^2_1		d^2_2		d^2_3		d^2_4		d^2_5		d^2_6
Update2				a^2_0		a^2_1		a^2_2		a^2_3		a^2_4		a^2_5		a^2_6
Approx.				a_0		a_1		a_3		a_4		a_5		a_6		a_7
Detail				d_0		d_1		d_3		d_4		d_5		d_6		d_7

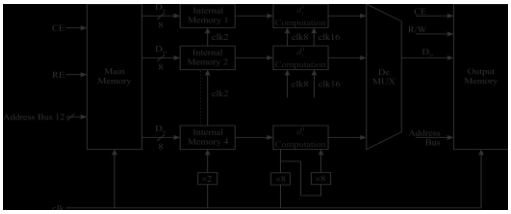

Fig 4. First stage parallel processing engines

In this work, Carry Look Ahead (CLA) Adder and Wallace Tree (WT) multiplier is used as they have less delay and regular structure. Figure 5 shows the four stages of pipelined parallel processing architecture with micro core engines to compute the predict and update samples.

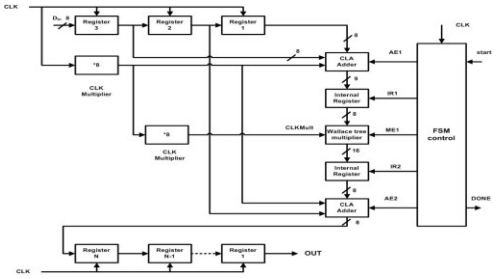

Fig 5 .Predict/update computation architecture with FSM

Computation of 1D DWT based on lifting approach in the proposed architecture is carried out using four parallel stages that operate on four input rows of image. The row operations are pipelined with five stages of computation units, with each unit consisting of micro core engines. Figure 6 shows the 1D DWT, with input image being decomposed into to sub band outputs of L and H. After 1D DWT the input image is reorganized into two bands of data as shown in Figure 6.

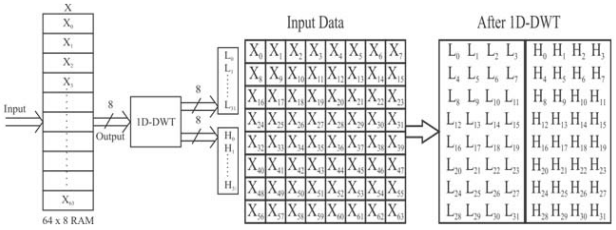

Fig 6.1D-DWT decomposition

B. 2D-DWT Architecture

Figure 7 shows the two level decomposition of 2D-DWT using proposed lifting scheme architecture. The output of 1D-DWT are stored in separate memory for computation of second level DWT and an intermediate memory is introduced that can feed data to second level DWT computation logic. The two stages of memory unit between 1D and 2D-DWT improves throughput by performing parallel processing operations of 1D and 2D-DWT. The input memory consists of L and H bands of coefficients that are read into the 2D processing module. Two 1D-DWT processes the L and H sub bands simultaneously controlled by clock input. Between 1D and 2D DWT processing two memories are introduced to synchronize data processing, the first memory stores the L and H sub bands, the second memory is designed to store the rearranged data as shown in Figure 7 prior to 2D-DWT processing. The intermediate clocks C5 and C6 control the read and write operations of intermediate memory. The four memories at the last stage of 2D DWT is controlled by C9 and C10 clock cycles that reorganizes the 2D output as shown in Figure 7. As there are two 1D DWT processing units that operate in parallel on each of the L and H sub band unit, the memory arrangement plays a vital role in data flow control. The 1D DWT architecture designed (shown in Figure 4) is used to process L and H samples, as there are four parallel processing units in 1D DWT, and there are N/2 columns to be processed the total number of clock cycles requires is (N/2*N/2)/4 + 48. Thus the computation of 2D DWT using proposed architecture is [(N*N)/4 + 48 + (N/2*N/2)/4 + 48)] clock cycles, and the proposed architecture requires multiple intermediate memories. For an input image of N x N x 8, after 2D DWT computation of 8 frames the input data is consists of four sub bands in each frame and there are eight frames as shown in Figure 8.

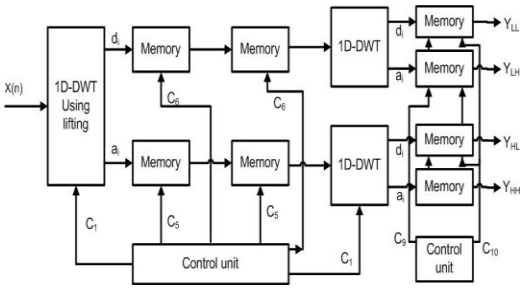

Fig.7 2D-DWT architecture

Figure 8 shows the four level sub bands obtained using the proposed architecture by introducing intermediate memories; pipelining and parallel processing is introduced for 2D-DWT computation.

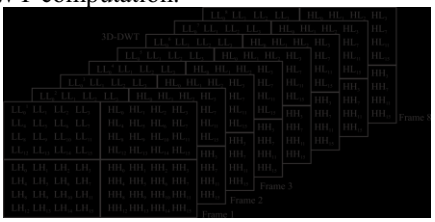

Fig .8 2D DWT of 8 input frames

III. 3D-DWT with proposed architecture

The 3D DWT is computed by performing 1D-DWT in the temporal domain. Figure 9 shows the 3D DWT computation process. The eight input frames each consisting

of N/2 x N/2 elements are processed using 1D – DWT, to produce two set of outputs. Thus all the four sub bands that are reorganized and processed in the temporal domain after DWT consist of 8 sub bands. Figure 10 shows the proposed 3D-DWT architecture with eight frames that are stored in separate memories and are processed simultaneously using eight different 2D-DWT processors.

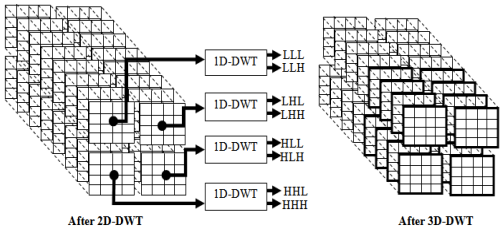

Fig 9. 3D DWT computation

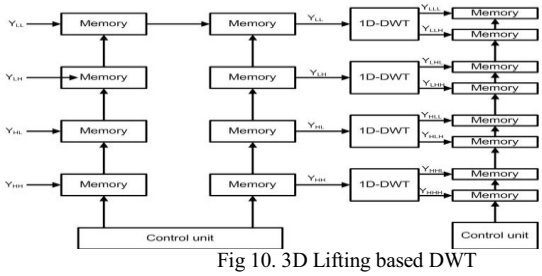

Fig 10. 3D Lifting based DWT

The eight input frames after 2D-DWT are decomposed in to four sub bands to compute 3D-DWT on all the decomposed sub bands. The input needs to be rearranged as shown in Figure 9. The output frames of 2D-DWT, the third level DWT is to be computed on each of the sub band of eight frames. The components LL_0^1 which is the first frame and LL_0^2 of the second frame and LL_0^3 of the third frame and so on till LL_0^7 of eight frame are grouped and stored in separate memory. Similarly, HL, LH, HH components of all eight frames is regrouped in to separate memories. These regrouped components are processed using four 1D-DWT process as shown in Figure 10. The 3D output decomposes the N x N x 8 input frame in to eight sub bands of N/4 x N/4 x 4 components representing LLL, LLH, LHL, LHH, HLL, HLH, HHL and HHH.

IV. RESULTS AND DISCUSSIONS

HDL code for the proposed model is developed in Verilog along with a test bench for functional verification. The input image consisting of group of frames are stored in an input file and the Verilog code developed with the test bench is interfaced with the text file storing the image. The test bench reads the input image files and sends the data pixel to 3D DWT engine for DWT decomposition. The test bench reads eight image files in parallel and feeds the eight input ports simultaneously. The 3D DWT decomposes the input images in to eight low pass and high pass filter combinations as LLL, LLH, LHL, LHH, HLL, HLH, HHL and HHH coefficients. Each combination of 3D DWT coefficients is stored in separate output files by image file writer. Figure 11 shows the block diagram of the test bench for validation of proposed 3D DWT architecture.

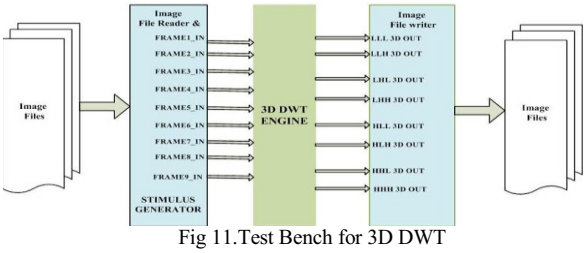

Fig 11.Test Bench for 3D DWT

The functionally correct HDL code is synthesized using Xilinx ISE targeting Virtex-5 FPGA device. The synthesis results obtained are captured and discussed.

The Virtex-5 device consisting of 49645 LUTs and 3456 memory units, for 3D DWT processing only 51% and 13% of resources have been utilized. Suitable constraints have been applied for speed optimization and it is found that the proposed 3D DWT architecture operates at maximum frequency of 373 MHz and hence is suitable for high speed applications. Table 3 shows the comparison of proposed architecture with references.

```
Device utilization summary:
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Selected Device : 5vlx155tff1136-3


Slice Logic Utilization:
 Number of Slice Registers:            38308  out of  97280    39%
 Number of Slice LUTs:                 49645  out of  97280    51%
    Number used as Logic:              46189  out of  97280    47%
    Number used as Memory:              3456  out of  26240    13%
       Number used as SRL:              3456

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:   52854
    Number with an unused Flip Flop:   14546  out of  52854    27%
    Number with an unused LUT:          3209  out of  52854     6%
    Number of fully used LUT-FF pairs: 35099  out of  52854    66%
    Number of unique control sets:      2761

IO Utilization:
 Number of IOs:                          237
 Number of bonded IOBs:                  237  out of    640    37%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                 2  out of     32     6%
```

Fig12. Area utilization report of 3D DWT

```
Timing Summary:
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Speed Grade: -3

   Minimum period: 2.676ns (Maximum Frequency: 373.692MHz)
   Minimum input arrival time before clock: 1.865ns
   Maximum output required time after clock: 2.878ns
   Maximum combinational path delay: No path found
```

Fig 13.Timing summary

The processing speed can be further improved by design of parallel processing architecture and Multiplier less architecture that can be incorporated at the first stage DWT and multicore engines respectively. Power dissipation for the proposed architecture is found to less than 1W, the power dissipation is due to the presence of large intermediate memories

TABLE III Proposed Architecture Specifications comparison with other implementations.

	Q.Dai et al [16]	J.Xu et al [14]	Z.Taghavi et al[15]	Anirban et al[5]	proposed
Memory Requirement	$4N^2$ +896N+968*2 (spatial+temporal)	$5N^2$ (only temporal)	$5N^2$ fast &few slow (only temporal)	$5N^2$(temporal)+5N(spatial)	$N^2+(N/2)^2$ $(N/4)^2$
Memory referencing at fixed FPS (i o/T)	-	5 ip/T, 5op/T	5 ip/T, 5op/T	5 ip/(2T), 5op/(2T)	5 ip/T, 5op/T
Throughput	-	1res/cycle	1res/cycle	2 res/cycle	1res/cycle
1 Level computational latency		$4N^2$ cycles	$4N^2$ cycles	($2 N^2$) cycles	2N cycles
Operating frequency	-	-	-	321MHz(Xilinx FPGA xc4vfx140)	373 MHz(Xilinx FPGA Virtex-5)
Area	-	-	-	1825 slices	49645 slices
Hardware utilization	-	-	-	100%	51%(only for DWT)
GOP	32(max)	Infinite	Infinite	Infinite	Infinite
Filter bank	For D-9/7	D-9/7	For D-9/7	D-9/7	D-9/7
Design type	Complete 3D	Temporal processor	Temporal processor	Complete 3D	Complete 3D
Number of levels	-	-	-	1	1

V. CONCLUSION

3D DWT computation is a complex process with large video frames that need to be compressed. Lifting scheme reduces the computation complexity, to improve the processing speed of sub band computation micro core engines are designed that operate in parallel. A parallel processing architecture is designed to process four rows in parallel thus reducing the processing delay, the pipelined architecture improves the throughput of 3D DWT computation. The parallel processing architecture that computes DWT of all 512 rows in the first stage, the 2D DWT in the second stage and the 3D DWT in the third stage are pipelined by introducing intermediate memories to improve latency. The developed architecture is modeled using Verilog HDL and is validated on FPGA platform. In brief, Novel architecture for 3D-DWT is designed, modeled and implemented on FPGA. The modified architecture operates at maximum frequency of 373 MHz. The architecture is hardware efficient and low power application. Where the maximum power consumption is 1W out of which the quiescent power 673mW.

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