A Low Power MICS Band Phase-Locked Loop for High Resolution Retinal Prosthesis

Jiawei Yang, Member, IEEE, and Efstratios Skafidas, Senior Member, IEEE

Abstract—Ultra low power dissipation is essential in retinal prosthesis and many other biomedical implants. Extensive research has been undertaken in designing low power biomedical transceivers, however to date, most effort has been focused on low frequency inductive links. For higher frequency, more robust and more complex applications, such as Medical Implant Communication Service (MICS) band multichannel transceivers, power consumption remains high. This paper explores the design of micro-power data links at 400 MHz for a high resolution retinal prosthesis. By taking advantage of advanced small geometry CMOS technology and precise transistor-level modeling, we successfully utilized subthreshold FET operation, which has been historically limited to low frequency circuits due to the inadequate transistor operating speed in and near weak inversion; we have implemented a low power MICS transceiver. Particularly, a low power, MICS band multichannel phase-locked loop (PLL) that employs a subthreshold voltage controlled oscillator (VCO) and digital synchronous dividers has been implemented on a 65-nm CMOS. A design methodology is presented in detail with the demonstration of EKV model parameters extraction. This PLL provides 600-mV$_{pp}$ quadrature oscillations and exhibits a phase noise of $-102$ dBc/Hz at 200-kHz offset, while only consuming 430-$\mu$W from a 1-V supply. The VCO has a gain ($K_{VCO}$) of 12 MHz/V and is designed to operate in the near-weak inversion region and consumes 220-$\mu$A DC current. The designed PLL has a core area of 0.54 mm$^2$. It satisfies all specifications of MICS band operation with the advantage of significant reduction in power which is crucial for high resolution retinal prosthesis.

Index Terms—Biomedical implants, low phase noise, Medical Implant Communication Service (MICS), multichannel, phase-locked loop (PLL), retinal prosthesis, subthreshold operation, super-low power.

I. INTRODUCTION

Implantable communication devices are important components for medical prostheses. Biomedical transceivers require low power consumption, since batteries are undesirable due to their limited lifetime and changing usually requires surgery. In these applications power is preferably acquired by wireless coupling [1], [2]. Moreover, these transceivers are usually preferred to be fully integrated on a single chip for easier surgery and encapsulation for better biocompatibility. Many biomedical telemetry systems have used very short-range magnetic (inductive) links [3]–[5]. These systems require close coupling between the external unit and implanted device and can be easily affected by electromagnetic interference (EMI), which presents a risk to patient safety and medical effectiveness due to the increasing usage of electromagnetic energy radiating devices such as cell phones and security systems. To overcome these limitations, more robust and more complex technologies, such as Medical Implant Communication Service (MICS) band (402–405 MHz with 10 channels) operation, have been recommended worldwide [6]–[10]. The MICS band is considered well suited for medical service for several reasons. One being that the 402–405 MHz signals have reasonable propagation characteristics in human body [11], [12]. In addition, equipment operating in the 402–405 MHz band can fully satisfy the requirements of MICS, achieving a good trade-off between size and power. Furthermore, the use of the MICS band does not pose a significant risk of interference to other radio within or close to this band [6]–[10].

Recently, some low power transceivers (either super-heterodyne or super-regenerative) working within the MICS band have been demonstrated in the literature [11], [13]–[19]. Although some of these use low power injection-locked [14] or frequency-calibrated [16], [17] oscillators to generate a local oscillation (LO) signal within the MICS band, they usually operate a single channel due to the elimination of an appropriate phase-locked loop (PLL). In [19], a digitally-controlled oscillator (DCO) was proposed which could be fine tuned within 1 kHz. A drawback of this tuning scheme was based on the knowledge of the exact tuning range and characteristics, which exhibit considerable process variation. Reliable multichannel operation is realized by incorporating a controllable PLL within the transceiver [11], [13], [15], [18]. However, these transceivers’ power consumption remains relatively high due to the PLL. Particularly, power dissipation of multichannel PLLs is more than 1 mW are reported. There has been considerable effort in designing low-power PLLs. An integer-N PLL operating using a 0.6-V supply, based on a quadrature VCO has been illustrated in [20] and, in [21], a 0.4–2.4-GHz PLL using a 0.5-V power supply is proposed with body-driven technique, in order to accommodate the low-voltage operation. Unfortunately, the supply voltage is usually set as a standard value that needs to be sufficient for all blocks in the system but may not be optimal for all blocks. Even if the PLL can work using 0.5 V, other digital or analog blocks may require higher supply voltage. A low global supply voltage may be undesirable in many practical systems.

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The authors are with National ICT Australia and the Department of Electrical and Electronic Engineering, The University of Melbourne, Victoria 3010, Australia (e-mail: jiayang@unimelb.edu.au).

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This paper explores the application of subthreshold operation, as a solution to lowering power dissipation, in the design of MICS band PLLs. Although the benefits of subthreshold design are well recognized, it has not been commonly adopted in practice due to the design model uncertainty and the transistor speed limitation (discussed in Section II-B). In this paper, we present a low power integer-N PLL using a subthreshold LC-tank VCO in MICS band implemented on a 65-nm CMOS, originally for an FSK transceiver in a high resolution retinal prosthesis (Bionic Eye) [22], [23], as shown in Fig. 1. As a very large number of pixels (electrodes) would be required for functional restoration of vision [24]–[26], reducing the power consumption of the data link becomes a critical issue since most of the energy should be reserved for stimulation and electrodes driving circuits. The power budget for our entire MICS transceiver is only 1 mW out of a total of 50 mW that is delivered from the extraocular unit [22]. The designed PLL, as a key component shared by both receiver and transmitter, only consumes 430-μW average power from 1-V supply, and can provide 600-μW quadrature output with a phase noise better than −102 dBc/Hz at 200-kHz offset, which is completely comparable with the achievements of previous strong inversion designs in the literature. The subthreshold VCO is designed to cover a frequency range of 392–412 MHz, while only drawing 220-μA bias current. This PLL satisfies all specifications of MICS band applications with the advantage of significant reduction in power consumption, which is crucial for high resolution retinal prosthesis and many other implantable devices.

II. LOW POWER VOLTAGE CONTROLLED OSCILLATOR DESIGN

A. Phase Noise Requirement for MICS Band VCO

The phase noise requirement for a MICS band VCO (after the PLL has been locked) is relatively relaxed. As demonstrated in Fig. 2 [27], while the signal \( P_{\text{sig}} \) is downconverted to an intermediate frequency (IF) by the LO \( P_{LO} \), the interference from adjacent channels \( P_{\text{int}} \) may be also downconverted to the same IF by the phase noise \( P_N \). Since the phase noise is a random process, the effective bandwidth \( P_{BW} \) is added to the total noise power calculation. The signal to noise ratio of the IF signal must meet the minimum SNR requirement

\[
P_{\text{sig}} + P_{LO} - (P_{\text{int}} + P_N + P_{BW}) > SNR_{\text{min}}. \quad (1)
\]
After rearrangement

\[ P_N - P_{LO} < P_{\text{sig}} - P_{\text{int}} - P_{\text{BW}} - SNR_{\text{min}} \]  \hspace{1cm} (2)

where \( P_N - P_{LO} \) represents the phase noise requirement in dB relative to the carrier power. For MICS band receivers, because of the limited distance and upper bound of EIPR, the dynamic range \( \left( \left| P(\text{sig}) - P_{\text{int}} \right| \right) \) is not high and is determined by the path loss at 2 m (around 30 dB [10]). If FSK modulation is used and the deviation of the two FSK tones is 50 kHz (i.e. \( f_{1,2} = f_c \pm 50 \text{kHz} \)), then the closest adjacent channel interferer is at 200 kHz away from the carrier. If a SNR of 10-dB is required by FSK demodulation [28] to obtain a bit error rate (BER) of 10^{-3} and additional 3-dB margin, we can write the phase noise at 200-kHz offset as

\[ P_{\text{noise}}[200 \text{ kHz}] < -30 - 10\log 1000 \text{ k} - 13 = -98 \text{ dBc/Hz} \]  \hspace{1cm} (3)

For our Bionic Eye application, the phase noise requirement is further relaxed since the transmission distance is only around 10 cm. The worst case power of the interference is at most at the same level as the desired signal. Therefore the required phase noise at 200 kHz from carrier is reduced to -68 dBc/Hz in our application.

When MICS transceivers are implemented with an integer-N type frequency synthesizer, the reference spurs, which are at multiples of 300 kHz, will appear in the VCO power spectrum and contribute to reciprocal mixing. The interference will also be downconverted by the spurious signal, which is considered as a single tone. Hence, we can write

\[ P_{\text{spur}} - P_{LO} < P_{\text{sig}} - P_{\text{int}} - SNR_{\text{min}} \]  \hspace{1cm} (4)

where \( P_{\text{spur}} - P_{LO} \) denotes the power of spur in dB relative to the power of carrier. The largest spur tone is located at 300 kHz from the carrier, therefore -43 dB spur attenuation at 300-kHz offset is required for the integer-N PLL in the design of a general MICS transceiver. In our special case of Bionic Eye, this requirement is reduced to -13 dBc due to the short communication distance.

### B. Subthreshold Operation and Design Methodology

It is commonly known that subthreshold device operation provides high transconductance for a given bias current. This property may be utilized to design extremely low power circuits. However, the increased transconductance efficiency exists at the expense of lower device transit frequency \( f_T \), which is defined as the frequency where the current gain of the device falls to unity. Therefore subthreshold designs have historically been associated with low frequency applications. Fortunately, \( f_T \) increases by 75%–100% in all regions of operation with each generation of scaling [29]. With 65 nm technology, we are able to drive the device into the weak inversion region to get the highest transconductance efficiency \( (f_m/ID) \) for 400-MHz operation.

In the EKV model, the drain current in weak inversion is given by [30]

\[ I_D = \frac{W}{L} I_0 e^{\tau} \left[ \frac{V_{GB} - V_{T0}}{nU_T} \right] \left[ e^{\left( \frac{-V_{SB}}{U_T} \right)} - e^{\left( \frac{-V_{DB}}{U_T} \right)} \right] \]  \hspace{1cm} (5)

where all the voltages are referred to the bulk. \( W/L \) is the device aspect ratio, \( V_{T0} \) is the equilibrium threshold voltage [30], [31], \( n \) is the subthreshold slope factor, \( U_T \) is the thermal voltage \( (25.85 \text{ mV at room temperature}) \) and, \( I_0 \) is defined in the EKV model as unary specific current, which represents the characteristic current for the device that has an unity aspect ratio \( (W/L = 1) \) in the center of moderate inversion. Equation (5) reveals that the drain current exhibits an exponential dependence on the gate voltage and source (or drain) voltage in “subthreshold” conduction. In this region, the drain current is mainly diffusion current and the device works like a bipolar transistor.

In fact, the drain current of a given device in any region of operation may be normalized to \( I_0 \), producing the inversion coefficient \( IC \), which provides a measure of the degree of inversion for a given device bias condition and is given by [30]

\[ IC = \frac{I_D}{I_0}. \]  \hspace{1cm} (6)

\( IC = 1 \) represents the center of moderate inversion, while \( IC < 0.1 \) indicates weak inversion and \( IC > 10 \) signifies strong inversion. From weak inversion to the center of moderate inversion, there is an intermediate state where the transistor behavior is still close enough to that in weak inversion. This area, near-weak inversion region, is defined with an upper-limit \( IC \) of around 0.5 [32]. It can be shown that when \( IC < 1 \), the device gate voltage must be lower than the threshold \( V_{T0} \) according to (5) and (6). We call it subthreshold operation.

The EKV model parameters \( n \) and \( I_0 \) are extracted using curve fitting. \( n \) was directly obtained from the \( I_D = f(V_{GB}) \) curve. \( I_0 \) was extracted in strong inversion region from the curves simulated by BSIM model, for it is considered correct in strong inversion. A standard approach is to plot \( \sqrt{I_D} = f(V_{SB}) \) function while keeping the gate voltage unchanged. The saturation drain current in strong inversion is approximated as [33]

\[ I_D = \frac{I_0 W}{4U_F^2} (V_P - V_{SB})^2 \]  \hspace{1cm} (7)

\(^1\) The threshold voltage of a MOSFET is defined as the gate voltage where an inversion layer (a “channel”) forms under the gate oxide between the source and drain. It is modeled differently in different MOSFET models, but is generally a point between weak inversion and strong inversion operation.

\(^2\) EKV model defines the gate threshold voltage \( V_{TB} \) as a function of the channel potential \( V_{CB} \). \( V_{T0} \) is the particular value of \( V_{TB} \) when \( V_{CB} = 0 \).

\(^3\) The drain current can be decomposed into two components: a forward current \( I_F \) and a reverse current \( I_R \). \( I_F \) depends on \( V_{GB} \) and \( V_{SB} \) whereas \( I_R \) depends on \( V_{GB} \) and \( V_{DB} \). Refer to [30] for more details.
Fig. 3. Principle of the determination of the specific current from $\sqrt{T_D} = f(V_{GS})$ curve.

TABLE I

<table>
<thead>
<tr>
<th>Device Type</th>
<th>$n$</th>
<th>$I_0$ [nA]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Regular NFET</td>
<td>1.49</td>
<td>252</td>
</tr>
<tr>
<td>Low $V_T$ NFET</td>
<td>1.40</td>
<td>261</td>
</tr>
<tr>
<td>High $V_T$ NFET</td>
<td>1.38</td>
<td>249</td>
</tr>
<tr>
<td>Regular PFET</td>
<td>1.50</td>
<td>132</td>
</tr>
<tr>
<td>Low $V_T$ PFET</td>
<td>1.59</td>
<td>137</td>
</tr>
<tr>
<td>High $V_T$ PFET</td>
<td>1.51</td>
<td>130</td>
</tr>
</tbody>
</table>

where $V_P$ is the pinch-off voltage in the EKV model and is constant for a fixed $V_{GB}$. It follows that

$$\frac{d\sqrt{T_D}}{dV_S} = \frac{I_0 W}{2U_T},$$

(8)

Hence, $I_0$ can be obtained from the strong inversion slope of the $\sqrt{T_D}$ versus $V_{GB}$ characteristic. Fig. 3 demonstrates an example $I_0$ extraction for a regular NFET of IBM cmos10lpe process. Table I is an example summary of the extracted $n$ and $I_0$ of various types of devices at minimum channel length for IBM cmos10lpe technology.4 $V_T0$ was also extracted, for design purpose, from plotting the $V_T$ versus $V_G$ characteristic by sweeping the gate voltage and reading the source voltage [33].

Fig. 4 plots the simulated transconductance efficiency ($g_m/I_D$ ratio) and $f_T$ against $IC$ for regular NFET in IBM cmos10lpe 65 nm process, which is the technology used in this work. It demonstrates that transconductance efficiency gradually saturates when the device enters the weak inversion region. This is particularly evident when $IC$ approaches 0.01, the device reaches maximum transconductance efficiency. In contrast, $f_T$ keeps decreasing when $IC$ becomes smaller. Thanks to the technology scaling, it can be found that in 65 nm process, $f_T$ is higher than 3 GHz when $IC = 0.1$ and this is maintained above 400 MHz even when $IC$ approaches 0.01. This fact is the basis of the subthreshold circuits design at MICS band.

Fig. 5 compares the $g_m/I_D$ ratios of regular NFETs with different channel lengths in weak and moderate inversion. It can be seen that longer lengths provide more transconductance in subthreshold, since the longer devices have more ideal subthreshold slope factor (closer to 1). However, using longer devices in or near weak inversion would more likely result in impractical large devices (large $W/L$) in a situation when relatively large $g_m$ is desired. Also, one can predict that the transconductance efficiency improvement reduces as the channel becomes longer. Therefore, minimum channel length (60 nm) is used in this work. Fig. 6 plots the $g_m/I_D$ ratios of different types of FETs with minimum length in weak and moderate inversion regions for the subthreshold circuits design in this work. Equipped with $g_m/I_D$ methodology, the analog design procedure could be simplified as follows: once the target $g_m$ is set, one could determine the amount of DC bias current that is required in the targeted region, as well as the desired device aspect ratio ($W/L$) for the given value of $IC$. Then one could determine the device channel length and width respectively based on area requirement. This design procedure is especially useful in subthreshold

4Corrections have been made to $n$ and $I_0$ values. We highlight the corrections here to draw the reader’s attention to the original errors in [23].
where the transconductance efficiency is nearly constant and the simulated $g_m/\beta$ values could be sufficiently accurate in (and near) weak inversion.

C. Low Power Quadrature VCO Realization

In [34], three different solutions for MICS band VCO in 0.18-µm TSMC CMOS process are compared. The first design is a 400-MHz LC tank loaded with a poly-phase filter. With 800-µA current, the measured phase noise at an offset of 160 kHz is $-98$ dBc/Hz. The VCO gain is approximately 15 MHz/V. The second solution is an 800-MHz LC tank with a master-slave divider. The phase noise in this case, which is $-97.7$ dBc/Hz at 160-kHz offset, is comparable to that of the 400-MHz LC tank, however the power consumption is much higher due to the use of the divide-by-2 divider. In addition, although a similar VCO gain of 17 MHz/V is achieved, the linear turning range of the VCO is much less compared to the 400-MHz design. The last design consists of a four-stage differential ring VCO. With much lower power consumption and smaller die area, the ring VCO however has a poor phase noise. The simulated phase noise is $-82$ dBc/Hz at 160-kHz offset and the measured value is further degraded. This level of phase noise may be acceptable for the Bionic Eye device. However, in order to make our design widely usable for general MICS applications, a better phase noise is desired (refer to Section II-A). Therefore ring VCO architectures are avoided in this work.

In this paper, a 400-MHz LC tank architecture is adopted for low power VCO design. The current-reuse topology, which uses nMOS-pMOS cross coupled pairs, is chosen as the VCO core to save power and is shown in Fig. 7. The VCO’s one single-ended output swing is transformed to a square wave through two inverters in the PLL loop, and its differential output is split to quadrature signals via a passive single stage poly-phase filter [34]. The input impedance of the poly-phase filter is maximized by carefully choosing the resistor and capacitor values, while keeping the capacitor large enough compared to parasitic capacitance, in order not to deteriorate the I-Q mismatch. The inductor value of the LC tank is made as large as possible for maximum oscillation amplitude. Two 25.8-nH inductors are connected in series to form a total inductance of 51.6 nH. The simulated quality factor for the cascade inductors is 7.4. The required $g_m$ that satisfies the unity loop gain at oscillation frequency is given by (10) as 1.75 mS

$$G_m \geq \frac{1}{\omega L Q_L}$$  \hspace{1cm} (10)$$

where $R_p$ models the total losses of the tank and $Q_L$ is the quality (Q) factor of the tank inductor. Note that here we do not consider the losses of the tank capacitors and varactors since they have much higher Q than the inductor at 400 MHz, also we ignore the parasitics from the active circuit itself. In practice, a closed loop gain of $2 \sim 3$ is often used to ensure sustained oscillation. In this design, the required $g_m$ is set to be 3.5 mS. Note that the actual $g_m$ requirement for each CMOS pair (nMOS pair or pMOS pair) is still 1.75 mS since using both nMOS and pMOS pair gives double amplification.

According to Fig. 6, suppose the maximum achievable $g_m/\beta$ ratio is 25 average for the nMOS and pMOS pairs in weak inversion, then the minimum required DC tail current is only 140 µA. However, since the tail current directly determines the oscillation amplitude and larger LO amplitude is preferred at the mixer for better gain and noise figure, the tail current is chosen to be 220 µA, providing 300-mV quadrature oscillation output voltage swing. Since $g_m/\beta$ ratio is constant in weak inversion, a fixed drain current is required to maintain the device $g_m$. On the other hand, with constant current, the $g_m$ will remain unchanged across process corners since $g_m/\beta$ ratio is invariant with process variation. Therefore, a fixed tail current is critical for the subthreshold VCO to maintain sufficient $g_m$. A current bias should be used in practice for the tail current source.

A pair of nCap varactors (NFET in N-well) are configured to give a VCO gain of 12 MHz/V. To calibrate for process and temperature variations, a 3-bit controlled capacitor bank is connected to the tank. Except for the current source M5, low-threshold (LVT) devices are chosen for all other transistors (M1 ~ M4) in the VCO core. This is to accommodate the use of a low supply voltage (1 V). M1 ~ M4 are finally configured in the near-weak inversion region for sufficiently high transconductance efficiencies but at the same time, avoiding impractically large device sizes. Table II lists key device dimensions/values and inversion coefficients in this design.

III. LOW POWER MICS BAND INTEGER-N PLL

The proposed PLL architecture in this work is demonstrated in Fig. 8. The PLL consists of an LC VCO, a synthesized digital divider, a dead-zone-free phase frequency detector (PFD), a charge pump (CP), and a third-order passive loop filter. The reference frequency comes from a 300-MHz MEMS resonator (divided by 1000), which is not described in this paper.

A. Phase Frequency Detector and Charge Pump Design

A TSPC (true-single-phase clock) D-Flip-Flop [35], as shown in Fig. 9, is chosen for the PFD design. The PFD built with this
TABLE II

<table>
<thead>
<tr>
<th>Device Name</th>
<th>Dimension/Value</th>
<th>Inversion Coefficient</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1,2</td>
<td>60µ/60n</td>
<td>0.4</td>
</tr>
<tr>
<td>M3,4</td>
<td>225µ/60m</td>
<td>0.2</td>
</tr>
<tr>
<td>M5</td>
<td>30µ/600m</td>
<td>16</td>
</tr>
<tr>
<td>L1,2</td>
<td>25.8nH</td>
<td>-</td>
</tr>
<tr>
<td>C1</td>
<td>2pF</td>
<td>-</td>
</tr>
<tr>
<td>C2,5</td>
<td>200nF</td>
<td>-</td>
</tr>
<tr>
<td>C3,6</td>
<td>100nF</td>
<td>-</td>
</tr>
<tr>
<td>C4,7</td>
<td>50nF</td>
<td>-</td>
</tr>
</tbody>
</table>

DFF does not exhibit sensitivity to the duty cycle variations, dead-zone and has unlimited detection range [35]. The charge pump schematic is shown in Fig. 10. This charge pump adopts a modified cascode current mirror architecture with a servo amplifier (op-amp) that forces $V_C$ equal to $V_Y$ [35]. M1, M4 are used as current switches and can also work as source degeneration resistors when they are turned on. M2, M3 can work as a bumper that absorbs supply turbulences and reduces switching charge injections (clock-feedthrough). The current in the second branch, which consists of M5 ~ M8, mirrors the reference current $I_{cp}$. The servo amplifier is very important since it makes the charge and discharge currents match, i.e., $I_{up} = I_{dn} = I_{cp}$. After PLL has been locked, there are still periodic $I_{up}$ and $I_{dn}$ current pulses due to up and down reset clock signals from the PFD. By employing this servo amplifier, $I_{up}$ and $I_{dn}$ are ideally canceled out and there would be no small periodic current variations. The power consumption of the servo amplifier is also minimized by operating it in weak inversion. A 30-pF ncap (NFET in n-well) capacitor is connected to the gates of M3, M7 and M11 in order to suppress the clock-feedthrough from the switch M4. Fig. 11 shows the I-V characteristics of the charge pump when the reference current is set to be 80 µA. Although the current values may deviate from 80 µA, $I_{up}$ and $I_{dn}$ are perfectly matched when the output voltage is within the range of 200 mV ~ 900 mV (when M2, M3 are in saturations). In PLL design, the deviations of output currents from the reference current are normally tolerable to certain extent while having the exact values of output currents matched is far more important. Therefore, the PLL is expected to perform well as long as the output voltage range, i.e., VCO control voltage range is kept within 200 mV ~ 900 mV.

The timings of the charge and discharge currents are also critical in order to eliminate the periodic current. Switch M4 is normally slower than Switch M1 due to slower switching response of PMOS devices as compared to NMOS devices. Buffers of proper sizes are required to be placed in between the PFD and CP, as illustrated in Fig. 12, in order to shorten the conducting time of both M1 and M4 and also to balance the propagation delays of the up and down clocks ($V_{up}$ and $V_{dn}$) at SW1 and SW2. Since switch M4 (30µ/60n) is three times wider than M1 (10µ/60n), it normally requires bigger buffers. In this work, we
applied a different but effective strategy, in which the same size but different number of buffers are used for M4 and M1. The buffer is simple inverter, consisting of a PFET and NFET. This size of buffer can easily drive both M4 and M1 with only slightly conducting time difference. Meanwhile, the number of buffers before M4 is one less than that before M1, therefore M4 conducts earlier than M1, which compensates the slower switching time. Fig. 13 shows the matched and as well as the matched and when there is no phase error at the PFD inputs. Fig. 14 demonstrates the detection range of the PFD and CP combination operating at 300 kHz. The average current in one cycle is linear with in the range of to . It also can be seen that no dead zone exists and is close to zero when is zero.

\[ F_{\text{div}} = F_{CH}(NP + S) \] (11)

where N, P and S represent the count numbers of the dual-modulus pre-scaler, P-counter and S-counter respectively. Now the channel bandwidth equal to 300 kHz, and choosing , and would cover 400.8 MHz to 405 MHz band.

The 10/11 dual modulus pre-scaler is implemented using a 5-stage twisted ring counter. A 5-bit synchronous up-counter that has parallel-load capability is used as the S-counter. As shown in Fig. 15, a two-input multiplexer is inserted before each DFF input. One input of the multiplexer provides the normal counting operation. The other input is a data bit that can be loaded directly into the flip-flop. In every counting cycle, S-counter counts starting from “”. When the count is equal to 20, it disables itself until being reset by the P-counter. Notice that in our channel selection, hence will always be zero and can be tied to the ground directly. The same type of synchronous counter is used as the P-counter. The 8-bit P-counter does not disable itself. Instead, it clears itself and re-counts from 0 automatically when it reaches 132. The use of synchronous counters greatly reduce the accumulation of the jitter, which is a known disadvantage of the asynchronous counter.

C. Loop Filter Design

The loop filter is a critical block that determines the PLL performance, such as phase noise performance, settling time and spurious tones suppression. Loop filters can be realized in forms
of either active and passive filters. Active filters require additional power consumption and noise rejection. Hence, a passive filter is employed in this design and is shown in Fig. 8. An additional filter (R2 and C3) is added to a 2nd order loop filter to further suppress spurious tones. In this design, the PLL loop is a 4th order. The loop filter parameters are directly related to the PLL system parameters: natural frequency \( \omega_n \) and damping factor \( \zeta \), and hence determine the settling time \( T_s \) when a frequency step \( f_{\text{step}} \) is applied [35].

\[
\omega_n = \frac{-1}{\zeta T_s} \ln \left( \frac{\Delta f}{f_{\text{step}}} \right)
\]

where \( \Delta f \) is an acceptable frequency deviation indicating that PLL is locked at the new frequency. The values of \( \omega_n \) and \( \zeta \) determine the PLL loop bandwidth \( B_L \)

\[
B_L = \frac{\omega_n}{2} \left( 1 + \frac{1}{4\zeta} \right).
\]

The PLL loop bandwidth is an important design parameter. Increasing the loop bandwidth reduces the settling time and improves VCO phase noise while decreasing the loop bandwidth can reduce the noise transferred from the reference clock and frequency divider, hence improves the spurious tones suppression.

Unlike a 3rd order PLL loop, whose component values can be easily obtained by calculating a set of simple linear formulas [36], a 4th order loop has many alternative derivations in the determination of its components due to the extra pole. According to [37], the generic 4th-order loop filter transfer function can be written as

\[
F_{4th}(s) = \frac{1}{s \tau_2 \left( 1 + s \tau_3 \right) \left( 1 + s \tau_4 \right)}
\]

where \( 1/s \tau_2 \) is the low frequency gain; \( \tau_2, \tau_3 \) and \( \tau_4 \) are the time constants. We can designate \( \tau_4 \) for the additional pole, then the required value for \( \tau_4 \) is

\[
\tau_4 = \frac{1}{\omega_n} \sqrt{10^{\text{Att}[\text{dB}]/10} - 1}.
\]

\( \text{Att} \) is the additional attenuation required at the first spur tone \( \omega_s \). Other two time constants can be expressed in terms of loop phase margin \( PM \) and natural frequency \( \omega_n \).

\[
\tau_2 = \frac{\tan(PM) + \sec(PM)}{\omega_n}
\]

\[
\tau_3 = \frac{\omega_s \cos(PM) - n \omega_n (1 + \sin(PM))}{\omega_n [\omega_s (1 + \sin(PM)) + n \omega_n \cos(PM)]}
\]

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

Fig. 16 shows the die photo of the PLL, which was fabricated on a 65-nm CMOS chip using IBM cmos10p process. As a test chip, it is required to have not only the feasibility of measuring the whole PLL, but also the flexibility that VCO alone can be tested. Thus, there are testing pads surrounding VCO for its control voltage and compensation bits. Due to this reason, the layout of the PLL was not optimized. The area of the VCO core is 0.308 mm², and the area of other parts of PLL is about 0.22 mm². Taking out testing pads, the core area of the entire PLL could be compressed within roughly 0.54 mm². Source-

<table>
<thead>
<tr>
<th>TABLE III</th>
<th>OPTIMIZED LOOP FILTER COMPONENTS AND PLL LOOP PARAMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>17.26pF</td>
</tr>
<tr>
<td>C2</td>
<td>216.0pF</td>
</tr>
<tr>
<td>R1</td>
<td>1.499kΩ</td>
</tr>
<tr>
<td>C3</td>
<td>7.46pF</td>
</tr>
<tr>
<td>R2</td>
<td>238.8kΩ</td>
</tr>
<tr>
<td>Unity gain frequency</td>
<td>15kHz</td>
</tr>
<tr>
<td>Phase margin at unity gain</td>
<td>45.54°</td>
</tr>
<tr>
<td>Spur attenuation</td>
<td>50.28dB</td>
</tr>
</tbody>
</table>

where \( n = \sqrt{10^{\text{Att}[\text{dB}]/10} - 1} \). The loop-filter gain term \( \tau_1 \) is calculated as

\[
\tau_1 = \tau_0 \sqrt{1 + \frac{1}{\omega_n^2 \tau_2^2} \left( 1 + \omega_n^2 \tau_4^2 \right)}
\]

\[
\tau_0 = \frac{K_v K_r}{N \omega_n^2} \left( \tan(PM) + \sec(PM) \right).
\]

By comparing (14) with the filter transfer function derived from Fig. 8, one can obtain four equations

\[
R_1 C_2 = \tau_2
\]

\[
R_1 C_2 C_3 R_1 R_2 = \tau_1 \tau_3 \tau_4
\]

\[
R_3 C_2 (C_1 + C_2) + R_3 C_3 (C_1 + C_2) = \tau_1 (\tau_3 + \tau_4)
\]

\[
C_1 + C_2 + C_3 = \tau_1.
\]

Because there are five required quantities in four equations, there exists a range of valid solutions with no definite answer. The design procedure is as follows:

1) Set the phase margin, natural frequency (which determine the loop bandwidth) and spur attenuation goal.
2) Calculate all time constants and low-frequency gain terms.
3) Define acceptable value ranges for all passive components and use mathematic tools to find out the optimal solution within the defined range.

This design procedure can guarantee a stable loop while keeping sufficient suppression to the spurious tones. Alternatively, fast optimization program, which runs in a similar way as above procedure, can be performed by using some professional design tools. In this work, loop filter optimization is done by the PLL design guide available in Advanced Design System (ADS). Table III shows the optimized loop filter components and PLL loop parameters.
follower type of output buffers are included on-chip to assist with measurement. These test buffers have a voltage loss of about $-7.6 \, \text{dB}$ when they are connected to $50 \, \Omega$. They are only for testing purpose and are not desired in the actual application. The free-running VCO was tested alone before the entire PLL was measured. One of the differential I-channel (or Q-channel) output of the VCO was terminated with $50 \, \Omega$ with the other connecting to a spectrum analyzer. The measured output power is $-14 \, \text{dBm}$, which converts to a voltage swing of $63 \, \text{mV}$ at $50 \, \Omega$. It can be deduced that the oscillation amplitude is approximately $150 \, \text{mV}$ (300 mV differential) before the testing buffer. This oscillation amplitude is generally sufficient for a MICS band mixer, especially when the mixer is also designed working in subthreshold region [38].

The measured VCO tuning characteristics with 3-bit compensation is shown in Fig. 17. Although the differences among the output powers with different combinations of compensation bits are very slight, the control voltage is preferred to be kept within the range of $200 \sim 900 \, \text{mV}$ for the optimal working condition of charge pump (refer to Section III-A). With compensation, this VCO can cover about 20-MHz frequency range. This tuning range is determined by the capacitor values in the compensation capacitor bank. The frequency variation of an LC tank VCO is caused by the process variations of all capacitances and inductances in the tank, therefore the subthreshold VCO is not different from the strong inversion design in this matter. The designed nominal tuning range is $392 \sim 412 \, \text{MHz}$ at $37^\circ\text{C}$ (when the control voltage is $200 \sim 900 \, \text{mV}$). 100-times Monte Carlo simulation (process + mismatch) suggested a standard deviation of 7 MHz, as shown in Fig. 18. Within the standard deviation, the designed VCO can still cover the 400.8–405 MHz band. Larger value capacitors are desired for the capacitor bank in order to compensate for the $2\sigma$ or $3\sigma$ deviation. Worst-case corner analysis with a temperature range of $20\sim60^\circ\text{C}$ was also performed. In this analysis, all corner parameters were set to between $-3$ and $+3$ yields $\pm3\sigma$ variations in the skew parameters of the devices affected. At two extreme corners, as shown in Fig. 18, the frequency variations exceed $23 \, \text{MHz}$. To cover the worst cases, the compensation capacitor values need to be made three times larger to have a 60-MHz tuning range, which however may not be necessary. Because the VCO is highly sensitive to multiple independent process or model parameters which may be controlled by a single corner parameter. The worst-case setting of corner parameters may result in values that far exceed what is expected from the long-term manufacturing environment, which is best represented by the statistical Monte Carlo simulations. Taking multiple corner parameters to a $3$ value result in overly pessimistic values since the process parameters are not correlated.

The PLL was measured for all channels of both receiver and transmitter ($S = 6 \sim 20$). The results have proved that the PLL responds very well to channel select inputs, and there are almost no performance differences among all channels. Fig. 19 gives the step response of the PLL from a locked state to another locked state, which was taken from the “$V_{\text{time}}$” terminal of the VCO and was recorded by an oscilloscope, indicating a settling time of about 350 $\mu\text{s}$. Fig. 20 illustrates the PLL’s spectrum when it is locked at 402 MHz and 405 MHz respectively.
Fig. 20. Measured spectrum of the PLL locked at (a) 402 MHz and (b) 405 MHz, respectively, with 10-MHz span and 1-MHz resolution bandwidth.

Fig. 21. Measured phase noise. (a) The free-running VCO tuned at 402 MHz. (b) The PLL locked at 402 MHz.

with 10-MHz span and 1-MHz resolution bandwidth. Accurate measurements of the phase noise were obtained by a software package provided by KE5FX GPIB Toolkit, which controls the spectrum analyzer via GPIB cables. As illustrated in Fig. 21, the phase noise characteristic of the proposed subthreshold VCO is very similar to that of a traditional VCO. The noise sources are mainly the flicker noise and the shot noise (dominant in subthreshold MOSFET [39], [40]). The flicker noise in NFET is actually not dependent on gate bias while the flicker noise in PFET is less in subthreshold than in strong inversion [41]. The shot noise in subthreshold saturation is modeled as [39], [40]

\[ I_{ns}^2 = 2qI_D \]  \hspace{1cm} (24)

where \( q \) is the charge on the electron and \( I_D \) is the drain current. Therefore in subthreshold operation, the less the current drawn by the VCO, the less the shot noise it exhibits. In strong inversion, the thermal noise dominates and is modeled in most of the literature as

\[ I_{th}^2 = 4KT \frac{q \mu m}{3} \]  \hspace{1cm} (25)

For this LC tank VCO design, one can actually compare the shot noise in subthreshold and the thermal noise in strong inversion. Same transconductance (\( g_m \)) value can be used in both cases. Suppose the \( g_m / I_D \) ratio is 25 in weak inversion and given that \( q = KT / U_T \), (24) can be re-written as

\[ I_{ns}^2 = 3KT g_m \]  \hspace{1cm} (26)

This shot noise current is only slightly bigger than the thermal noise current in strong inversion (25). Taking into account the fact that the flicker noise is less in subthreshold, the noise performance of this subthreshold VCO is expected comparable with the achievements of strong inversion designs. The flat part in Fig. 21 at low frequency offset is probably due to the carrier frequency drifting of the free-running VCO. When the carrier frequency is 402 MHz, the phase noises at 200-kHz offset of
the free-running VCO and the locked PLL are $-99$ dBc/Hz and $-102$ dBc/Hz, respectively. The VCO’s phase noise was improved by the PLL, especially at low offset frequencies within the loop filter’s bandwidth (around 15 kHz). Note that the measurements were performed at the VCO’s single-ended output, therefore the actual phase noises of the differential oscillation signals would be better due to the rejection of the common mode noise from power supply and substrate. The phase noise improvement because of the “phase lock” can also be seen in Figs. 22(d) and 22(c), where the resolution bandwidth were 10 kHz and the span were 100 kHz for both cases. The free-running VCO’s spectrum already displays a noise-like signal, and its center has drifted apart from 402 MHz whilst the PLL’s spectrum still exhibits a nice peak at the carrier frequency with suppressed noise within the loop filter’s bandwidth, which indicates the PLL is locked. Note that there is still some low frequency noise coupled from the measurement environment showing in the spectrum since the resolution bandwidth was not set low enough. The phase noise of the PLL at 15-kHz offset can be read and approximately calculated as $-30 - 10 \log 10 \ k = -70$ dBc/Hz, where 10 kHz is the resolution bandwidth of spectrum analyzer. This is roughly consistent with Fig. 21. The clock feedthrough can be found in Fig. 22(a), which indicates the maximum feedthrough at 300-kHz offset is approximately $-45$ dBc.

This PLL not only achieves low power consumption by taking advantage of subthreshold operation, also achieves excellent phase noise performance because of the optimized designs of all components in the loop. To evaluate this work, a well known figure of merits (FOMs) [21], [42] is employed, as defined in (27) with trade-off parameters, including phase noise $L(\Delta\omega)$, power dissipation $P_D$, carrier frequency $\omega_0$, and offset frequency $\Delta\omega$. Table IV shows the comparison of this work with respect to the state-of-the-art reported in the literature.

$$FOM = L(\Delta\omega) - 20\log_{10} \left( \frac{\omega_0}{\Delta\omega} \right) + 10\log_{10} \left( \frac{P_D}{1 \text{ mW}} \right)$$

V. CONCLUSION

Developing an extremely low power PLL is crucial for the very-low-energy transceivers in the applications of retinal prosthesis and many other implantable biomedical devices. However, achieving super low power at microwatts is a very challenging target because power is directly related to the circuit...
performance, in terms of gain, noise and linearity. Even at relatively low frequencies, such as applied to the MICS band, multichannel PLLs that consume less than 1 mW have not been reported in the literature.

By utilizing precise subthreshold modeling and various other circuit-level energy-saving techniques, a low power MICS band PLL, which enables multichannel operations for the MICS band transceivers, was successfully designed and implemented in this paper.

Following the \( g_{m_0}/I_D \) design methodology, each building block was carefully designed to achieve low power consumption whilst having required performance characteristics. The PFD/CP was designed to have zero detection dead zone, and identical charge and discharge currents by using a servo amplifier in weak inversion; the loop filter was optimized with 3-bit compensation that accommodate for process variations, while consuming minimal power; the channel selection was achieved via synchronous digital dividers, which minimize the accumulation of the jitter. Overall, this PLL satisfies all the specifications and requirements for MICS band application with the advantage of significant reduction in power dissipation.

**REFERENCES**


Jiawei Yang (M’09) received the B.Eng. degree in electrical engineering from Zhejiang University, Hangzhou, Zhejiang, China, and the Ph.D degree in electrical and electronics engineering from the University of Melbourne and National ICT Australia, Victoria, in 2004 and 2011, respectively. From 2004 to 2007, he was an Electrical Engineer at Honeywell, China. Currently, he is a Research Fellow for the Center for Neural Engineering (CINE) at the University of Melbourne, focusing on designing electronics for high acuity retinal prosthesis and other biomedical implants. His research interests includes low power/high speed analog and mix-signal circuit design, integrated electronics for biomedical devices, and microelectromechanical systems (MEMS).

Efstratios Skafidas (M’98–SM’03) received the B.E. (Hons.), B.Sc., and Ph.D. degrees in electrical engineering from the University of Melbourne, Parkville, Australia. Since completing the Ph.D. degree in 1998, he has focused his research in the areas of novel nano-electronic systems, communication technologies, and smart antenna theory. His work has led to innovative new millimeter-wave communication systems on CMOS and has been the basis of new biomedical devices. His research is currently incorporated in multiple international communication standards and has led to the establishment of two startup companies. He is currently a Professor of nano-electronics and the Director of the Centre for Neural Engineering (CINE), The University of Melbourne, Parkville, Australia. He played an integral role in establishing CINE, an interdisciplinary center established to undertake research in neuroscience and neural diseases by drawing together Australias leading neuroscientists, neurologists, psychiatrists, chemists, physicists, and engineers.