LOW POWER AREA EFFICIEN ALU WITH LOW POWER FULL ADDER

S.Usha
Department of ECE
Chettinad College of Engineering and Technology
Karur, India

M.Rajendiran
Professor of ECE
Chettinad College of Engineering and Technology
Karur, India

A.Kavitha
Professor and Head of ECE
Chettinad College of Engineering and Technology
Karur, India

***Abstract*-This paper presents a low Power Area efficient ALU using XNOR logic. The 4bit ALU design is compared with various ALU implementation models with respect to their power consumption and area. ALU is an Arithmetic and Logic Unit, which performs arithmetic operation like ADD, SUB, PASS THROUGH, TWO'S COMPLEMENT, etc. and logic operation like AND, OR, EXCLUSIVE OR, EXCLUSIVE NOR, etc. We introduce a low power full adder, that consists of 8T which is generated using 3T XNOR logic and multiplexer. Full adder is the basic component for an ALU. By reducing the power of full adder, the ALU power also be reduced. Compared with Gate Diffusion Input Full Adder, 50% power reduced in the XNOR based Full Adder Technique. The simulation is carried out using cadence virtuoso 180nm technology, and compared with previous design of Gate Diffusion Input (GDI) technology. The result shows area efficient and low power consumption compared with Gate Diffusion Input technique.**

Keywords-ALU; Gate Diffusion Input technique; XNOR logic.

I. INTRODUCTION

Today all the VLSI circuits performs on low power with high speed. The arithmetic and logic unit operations are essential behavior for low power high speed application like digital signal processing, microprocessor, VLSI, microcontroller, ASIC, etc. ALU is an arithmetic and logic unit which behaves all arithmetic and logic operations. ALU constructed using full adder, 2x1 and 4x1 multiplexer circuits. The 1-bit full adder circuit ismapped using 3T XNOR techniques, 2x1 multiplexer and 4x1 multiplexer circuits has been designed using Gate Diffusion Input technique. The transistor count is reduced and power decay is also reduced correlated to GDI technique and 2T XOR techniques. This paper idolizes the approach of 3T XNOR procedure based full adder in the layout of Arithmetic and Logic unit.

The respite of paper is classified as pursues Section II explains the previous works. Section III consists of the justification of technique used in the present work. In the Section IV rationalizes the operation of arithmetic and logic unit design. Section V defines the simulation result and analysis. At the end conclusion is made in Section V.

II. PREVIOUS WORKS

The previous paper presents a Gate Diffusion Input technique (GDI), which is a approach for reducing the power and area. ALU operation can be performed by the 4x1 multiplexer, 2x1 multiplexer and full adder. GDI cell incorporate one PMOS and one NMOS, which view like an inverter, but it consists of three inputs and one output. 4x1 multiplexer, 2x1 multiplexer and full adder blocks are implemented using Gate Diffusion Input technique.

2x1 multiplexer based Gate Diffusion Input technique are implemented using two transistors and consumes the power of 1.394µW. 4x1 multiplexer based Gate Diffusion Input technique are implemented using six transistors and consumes the power of 2.987µW. Full adder based Gate Diffusion Input technique has 10 transistor and consumes the power of 10.190µW. ALU based GDI technique hasconsumed the power of 3.994mW. The low power full adder cell based on the XNOR logic consists of 66.32Pw.Based on the full adder implementation of sum using XOR-XNOR and COUT using NMOS-PMOS logic, which gives the improved conclusion in speed, Power and threshold loss problem.In the design of 1bit full adder consists of 6transistor with two inverter, which has consumes the power of 55.29pW.

Full adder based 14T consumes the power for ALU is 59.27pW. XNOR Technique based full adder is a new method for reducing the power with less area. VivechanaDubey and Ravimohansairam explained an arithmetic and logic unit optimized for area and power using GDI technique [11].

III. GATE DIFFUSION INPUT TECHNIQUE

GATE DIFFUSIONTECHNIQUE is an recentapproach in the VLSI, it is used to consume the power and reduce the area. It consists of three inputs and single output, the inputs are G, P, N.

The G is an common gate input, P represent S or DPmos input and N represents S or D Nmosinput.The G and N input is either '0' or '1', when P input is '1',it performs A'+B operation otherwise it performs AND operation. When N, P,

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G has either ‘0’ or ‘1’ input, it performs MUX operation. When N input is ‘0’, P input is ‘1’ and G has either ‘0’ or ‘1’, it performs NOT operation.

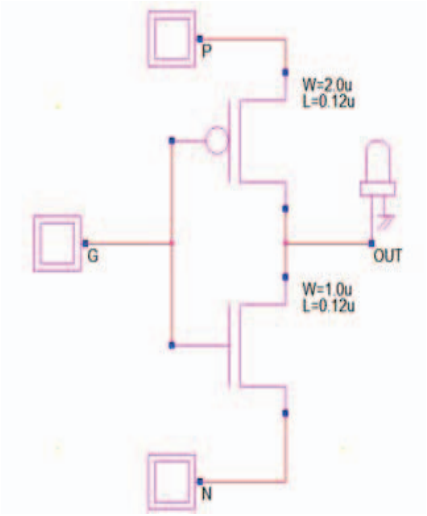

Fig. 1. Basic GDI Cell

A. GDI BASED 2X1 MULTIPLEXER

Multiplexer acts as an switch. Multiplexer has n selection line and 2^n input line. For 2x1 multiplexer, it consists of two inputs and one selection line. Based on the selection line, the output can be generated. Selectionswitch is associated to the gate, depending on the selection line, PMOS or NMOS can be ‘on’. When selection input is ‘0’, the PMOS will be ‘on’. When the selection line is ‘1’, the NMOS will be ‘on’.

TABLE I. LOGIC FUNCTIONS OF GDI CELL

S.No	N I/P	P I/P	G I/P	OUTPUT	FUNCTION
1	0	B	A	A’B	F1
2	B	1	A	A’+B	F2
3	1	B	A	A+B	OR
4	B	0	A	AB	AND
5	C	B	A	A’B+AC	MUX
6	0	1	A	A’	NOT

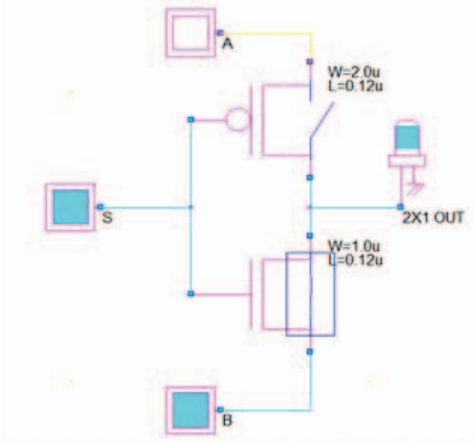

Fig. 2. 2x1 multiplexer based GDI technique

B. GDI BASED 4X1 MULTIPLEXER

4X1 Multiplexer consists of four inputs and two selection line. It has six transistors, depending on the two selection line, the output will be generated. When s0s1=’0’, then A input is taken as an output. When s0=’0’ and s1=’1’, then B input is given to the output. When s0=’1’ and s1=’0’, then C input is given to the output. When s0s1=’1’, then D input is taken as an output.

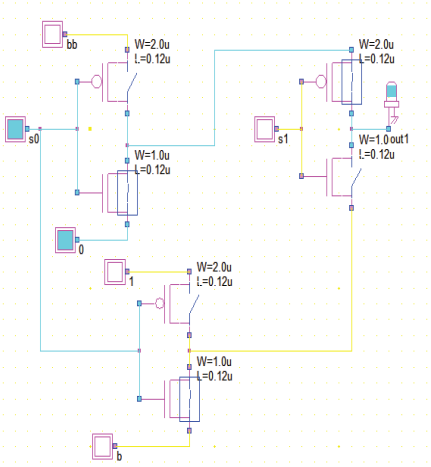

Fig. 3. 4x1 multiplexer based GDI technique

C. XNOR TECHNIQUE

XNOR gate is the basic architecture section for full adder circuit. The 3Transistor XNOR module consumes the less power than the XOR module. When A and B input is zero, it gives the output value as '1'. When A=0/1 and B=0/1, it gives the output value as '0'. When A and B input is one, then it gives the output value as '1'.

D. FULL ADDER BASED XNOR TECHNIQUE

Full adder based XNOR technique has 8T, it consists of two 3T XNOR module generates the SUM output and multiplexer generates the CARRY output. Full adder is a basic component for an ALU. Depending on the three input A, B, C, the sum and carry output can be generated. Full adder based XNOR technique consumes the power of 86.39pW.

E. DESIGN OF ALU USING LOW POWER FULL ADDER

An arithmetic and logic unit is a fundamental block for many processors. It performs many operations like addition, subtraction, XOR, XNOR, buffer, NAND, OR, etc. The 4 bit ALU operation can be implemented using eight 4x1 multiplexer, four full adder, four 2x1 multiplexer. Depends upon the three selection line s2, s1, s0, the arithmetic and logic operation can be performed**.**

The block of 4x1 multiplexer consists of four input, which is logic 0, logic 1, B and B'. Depends upon the s0 and s1 selection line, the desired output can be generated. These output can be indicate as the B. this acts as an 'B' input for the full adder. Then the full adder operation can be performed using XNOR logic and generates the sum and carry output.

The next stage of 4x1 multiplexer has the input of full adder sum, which is EXOR, EXNOR, AND and OR. Depends on the s0 and s1 selection line, the output can be generated. It acts as an input for the 2x1 multiplexer. Another input of 2x1 multiplexer is the full adder SUM output. Finally, the output stage of 2x1 multiplexer can be generated using s2 selection line.

TABLE II. OPERATIONS OF ALU

S2	S1	S0	OPERATIONS
0	0	0	Buffer
0	0	1	EXOR
0	1	0	EXNOR
0	1	1	OR
1	0	0	ADDITION
1	0	1	SUBTRACTION
1	1	0	BITWISE NAND
1	1	1	Inverter

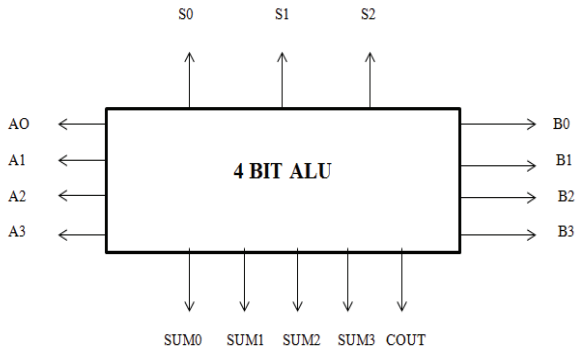

Fig. 4. Logo representation of ALU

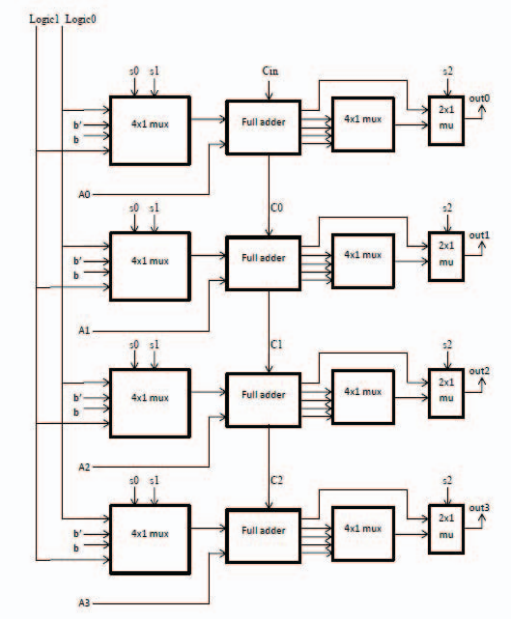

Fig. 5. Process of 4bit Arithmetic and Logic Unit

Multiplexer logic at the input stage consists of 4x1 multiplexer and 2x1 multiplexer. Depends upon the selection line of s0, s1 and s2, the output of full adder has been computed. Multiplexer logic at the output stage consists of 4x1 multiplexer and 2x1 multiplexer. Depends upon the selection line of s0, s1, and s2, the output of ALU has been computed. Input stage multiplexer consists of VDD, VSS, B and B'. The output stage multiplexer consists of EXOR, EXNOR, AND and OR input. Fig.8 shows input stage of multiplexer architecture and Fig 9 shows output stage of multiplexer architecture.

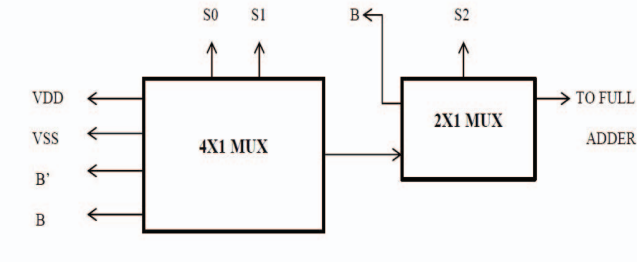

Fig. 6.

This paper presents a new technique of XNOR logic, to design the full adder for an ALU. In prior design of ALU, the full adder is resolved by Gate Diffusion Input technique which proven to have high power consumption and compared with XNOR logic. These new approach of XNOR logic gives excellent result then previous design in charge of power consumption, area as well as propagation delay.

Fig. 6. Arichitecture of multiplexer logic at the input stage

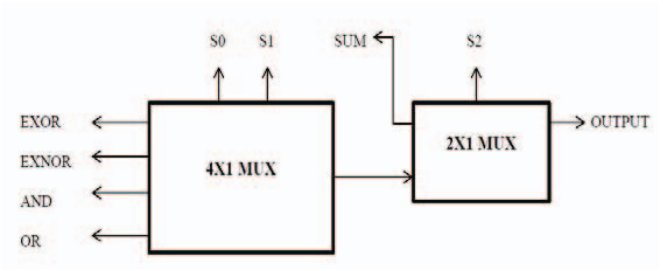

Fig. 7. Arichitecture of multiplexer logic at the output stage

The schematic of 4-bit ALU has been implemented using cadence virtuoso platform. It shows interface between the peripherals. Figure 10 describes the delineative look of ALU.

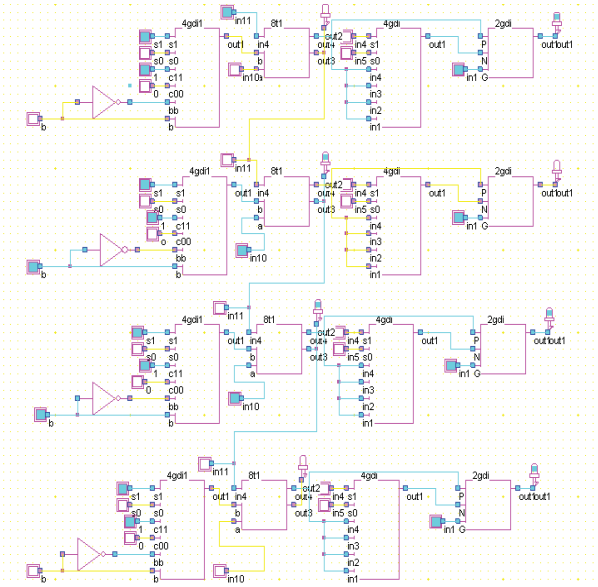

Fig.10. Delineative view of 4bit ALU

IV. SIMULATION RESULTS AND ANALYSIS

This chunk describes the execution of the prospectivelayout using cadence virtuoso platform on 180nm technology. The simulation results shows the output of 2x1 multiplexer, 4x1 multiplexer, full adder and complete 4-bit ALU is shown in figure 11,12,13 and 14**.** Fig 15 shows the bar chart for power consumption and number of transistor.

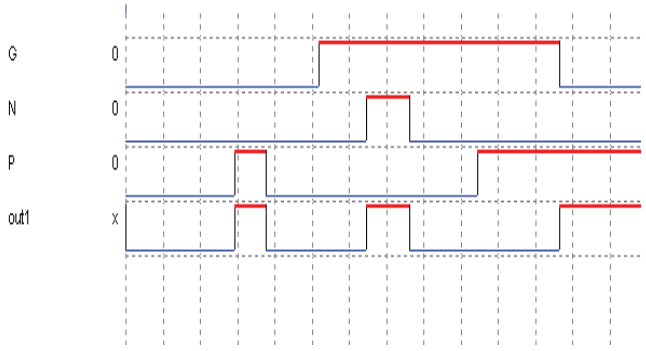

Fig. 8. Simulated output of 2x1 multiplexer

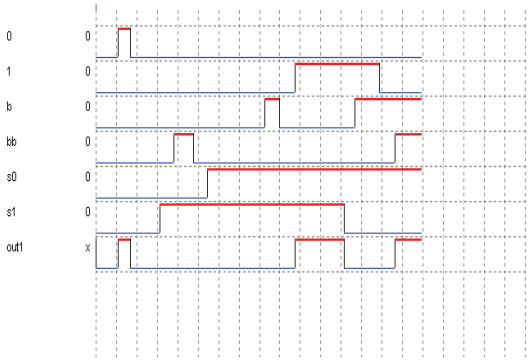

Fig. 9. Simulated output of 4x1 multiplexer

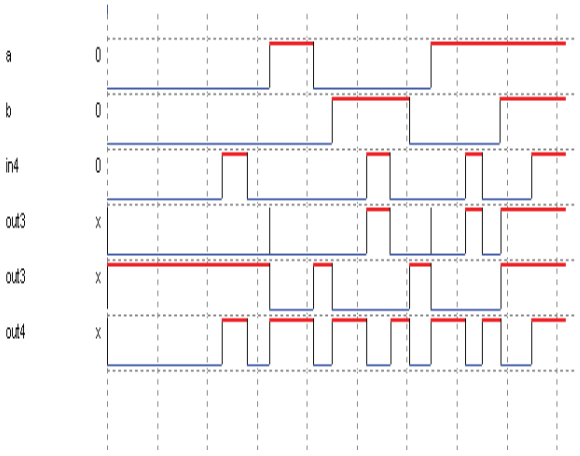

Fig. 10. Simulated output of 1bit full adder

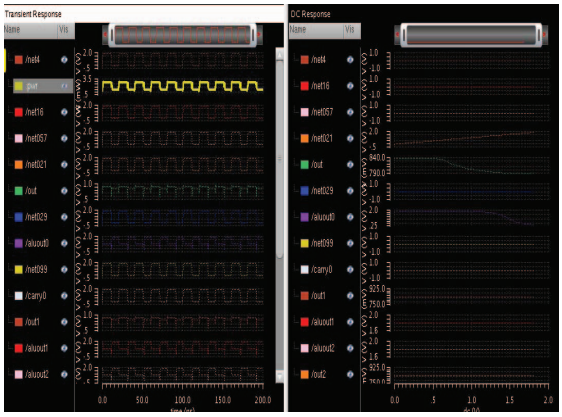

Fig. 11. Simulated output of 4bit ALU

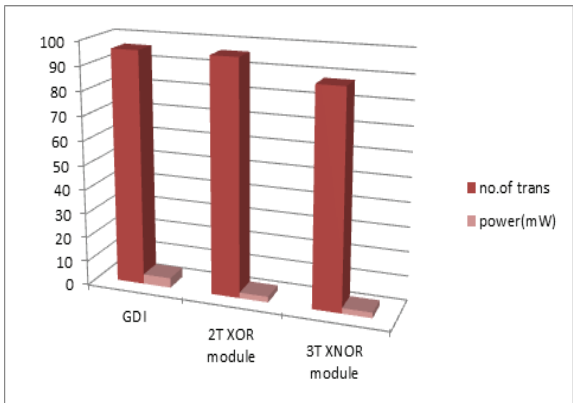

Fig. 12. Bar chart for power and no. of transistor

TABLE III. 4BIT ALU POWER CONSUMPTION

S.No	DESIGN	No. of Transistors	Power(mW)
1	ALU with GDI Technique	96	3.994
2	ALU with 2T XOR Module	96	2.308
3	ALU with 3T XNOR Module	88	2.250

V. CONCLUSION

This work presents a 4-bit ALU designed using Cadence Virtuoso 180nm technology for less area and low power with 3T XNOR full adder and Gate Diffusion Input(GDI) multiplexer. Various methods of multiplexer and full adder are implemented and compared. Compared with previous paper, it reduces the power and area to 44%. The 2x1 multiplexer and 4x1 multiplexer are designed using Gate Diffusion Input technique. Full adder based proposed technique consumes 10.190µW, but 3T XNOR technique consumes 8.639µW. Using these techniques, full adder power leads to reduce, therefore the ALU design also tends

to reduced. Power dissipation, Propagation delay and number of transistor are compared using GDI, PTL, 2T XOR and 3T XNOR technique.

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