Implementation of an Efficient Multiplier based on Vedic Mathematics Using EDA Tool

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Abstract*:- *A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. This paper presents a high speed 8x8 bit Vedic multiplier architecture which is quite different from the Conventional method of multiplication like add and shift. The most significant aspect of the proposed method is that, the developed multiplier architecture is based on Vertical and Crosswise structure of Ancient Indian Vedic Mathematics. It generates all partial products and their sum in one step. This also gives chances for modular design where smaller block can be used to design the bigger one. So the design complexity gets reduced for inputs of larger no of bits and modularity gets increased. The proposed Vedic multiplier is coded in VHDL (Very High Speed Integrated Circuits Hardware Description Language), synthesized and simulated using EDA (Electronic Design Automation) tool - XilinxISE12.1i. Finally the results are compared with Conventional multipliers to show the significant improvement in its efficiency in terms of path delay (speed). The high speed processor requires high speed multipliers and the Vedic Multiplication technique is very much suitable for this purpose.

Index Terms*:- *Architecture, Ripple Carry (RC) Adder, Multiplication, Vedic Mathematics, Vedic Multiplier (VM), Urdhava Tiryakbhyam Sutra

I. INTRODUCTION

Multipliers are extensively used in Microprocessors, DSP and Communication applications. For higher order multiplications, a huge number of adders are to be used to perform the partial product addition. The need of high speed multiplier is increasing as the need of high speed processors are increasing. Higher throughput arithmetic operations are important to achieve the desired performance in many real time signal and image processing applications. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications**.** In the past multiplication was implemented generally with a sequence of addition, subtraction and shift operations. Two most common multiplication algorithms followed in the digital hardware are array multiplication algorithm and Booth multiplication algorithm. Due to the importance of digital multipliers in DSP, it has always been an active area of research. Vedic mathematics is the name given to the ancient system of mathematics, which was rediscovered from the ancient Indian scriptures between 1911 and 1918 by Jagadguru Swami Sri Bharati Krisna Tirthaji (1884-1960), a scholar of Sanskrit, mathematics, history and philosophy. The whole of Vedic mathematics is based on 16 Vedic sutras, which are actually word formulae describing natural ways of solving a whole range of mathematical problems [1].

The paper is organized as follows. Section II describes the basic methodology of Vedic multiplication technique. Section III describes the proposed multiplier architecture based on Vedic multiplication and the generalized algorithm for NxN bit Vedic multiplier. Section IV describes the design and implementation of Vedic multiplier module in XilinxISE12.1. Section V comprises of Result and Discussion in which device utilization summary and computational path delay obtained for the proposed Vedic multiplier (after synthesis) is discussed. Finally Section VI comprises of Conclusion.

II. VEDIC MULTIPLICATION TECHNIQUE

The use of Vedic mathematics lies in the fact that it reduces the typical calculations in conventional mathematics to very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Vedic Mathematics is a methodology of arithmetic rules that allow more efficient speed implementation. It also provides some effective algorithms which can be applied to various branches of engineering such as computing.

A. Urdhva Tiryakbhyam Sutra

The proposed Vedic multiplier is based on the "Urdhva Tiryagbhyam" sutra (algorithm). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. It is a general multiplication formula applicable to all cases of multiplication. It literally means "*Vertically and Crosswise*". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Due to its regular structure, it can be easily layout in microprocessors and designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers.

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B. Multiplication of two decimal numbers 252 x 846

To illustrate this scheme, let us consider the multiplication of two decimal numbers 252 x 846 by Urdhva-Tiryakbhyam method as shown in Fig. 1. The digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and all other bits act as carry for the next step. Initially the carry is taken to be zero.

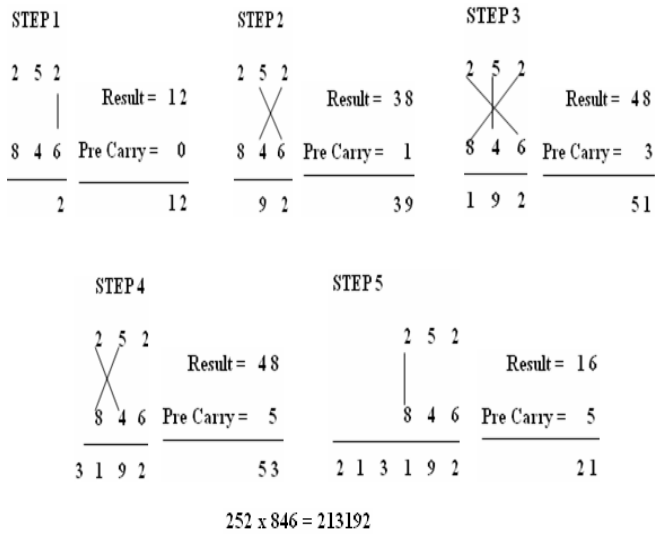

Fig. 1 Multiplication of two decimal numbers – 252 x 846

III. THE PROPOSED MULTIPLIER ARCHITECTURE

The hardware architecture of 2X2, 4x4 and 8x8 bit Vedic multiplier module are displayed in the below sections. Here, "Urdhva-Tiryagbhyam" (*Vertically and Crosswise*) sutra is used to propose such architecture for the multiplication of two binary numbers. The beauty of Vedic multiplier is that here partial product generation and additions are done concurrently. Hence, it is well adapted to parallel processing. The feature makes it more attractive for binary multiplications. This in turn reduces delay, which is the primary motivation behind this work.

A. Vedic Multiplier for 2x2 bit Module

The method is explained below for two, 2 bit numbers *A* and *B* where *A* = *a*1*a*0 and *B* = *b*1*b*0 as shown in Fig. 2. Firstly, the least significant bits are multiplied which gives the least significant bit of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. The sum is the third corresponding bit and carry becomes the fourth bit of the final product.

$s0 = a0b0;$ (1)

$c1s1 = a1b0 + a0b1;$ (2)

$c2s2 = c1 + a1b1;$ (3)

The final result will be *c*2*s*2*s*1*s*0. This multiplication method is applicable for all the cases.

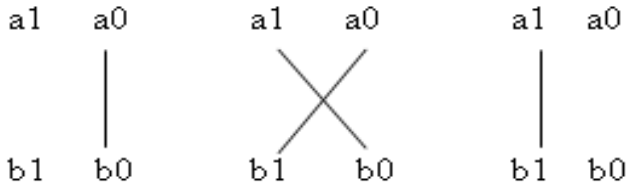

Fig. 2 The Vedic Multiplication Method for two 2-bit Binary Numbers

The 2X2 Vedic multiplier module is implemented using four input AND gates & two half-adders which is displayed in its block diagram in Fig. 3. It is found that the hardware architecture of 2x2 bit Vedic multiplier is same as the hardware architecture of 2x2 bit conventional Array Multiplier [2]. Hence it is concluded that multiplication of 2 bit binary numbers by Vedic method does not made significant effect in improvement of the multiplier's efficiency. Very precisely we can state that the total delay is only 2-half adder delays, after final bit products are generated, which is very similar to Array multiplier. So we switch over to the implementation of 4x4 bit Vedic multiplier which uses the 2x2 bit multiplier as a basic building block. The same method can be extended for input bits 4 & 8. But for higher no. of bits in input, little modification is required.

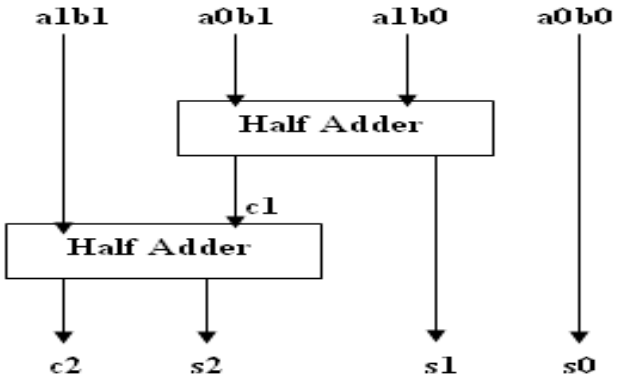

Fig. 3 Block Diagram of 2x2 bit Vedic Multiplier

B. Vedic Multiplier for 4x4 bit Module

The 4x4 bit Vedic multiplier module is implemented using four 2x2 bit Vedic multiplier modules as discussed in Fig. 3. Let's analyze 4x4 multiplications, say A= $A_3 A_2 A_1 A_0$ and B= $B_3 B_2 B_1 B_0$. The output line for the multiplication result is – $S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0$ .Let's divide A and B into two parts, say $A_3 A_2$ & $A_1 A_0$ for A and $B_3 B_2$ & $B_1 B_0$ for B. Using the fundamental of Vedic multiplication, taking two bit at a time and using 2 bit multiplier block, we can have the following structure for multiplication as shown in Fig. 4.

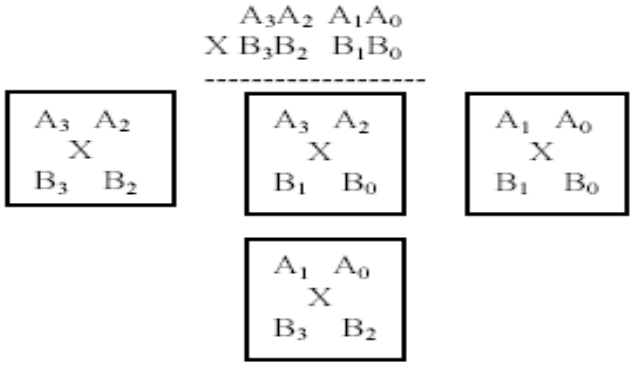

Fig. 4 Sample Presentation for 4x4 bit Vedic Multiplication

Each block as shown above is 2x2 bit Vedic multiplier. First 2x2 bit multiplier inputs are A_1A_0 and B_1B_0. The last block is 2x2 bit multiplier with inputs $A_3 A_2$ and $B_3 B_2$. The middle one shows two 2x2 bit multiplier with inputs $A_3 A_2$ & B_1B_0 and A_1A_0 & $B_3 B_2$. So the final result of multiplication, which is of 8 bit, $S_7 S_6S_5S_4 S_3 S_2 S_1 S_0$. To understand the concept, the Block diagram of 4x4 bit Vedic multiplier is shown in Fig. 5. To get final product ($S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0$), four 2x2 bit Vedic multiplier (Fig. 3) and three 4-bit Ripple-Carry (RC) Adders are required.

The proposed Vedic multiplier can be used to reduce delay. Early literature speaks about Vedic multipliers based on array multiplier structures. On the other hand, we proposed a new architecture, which is efficient in terms of speed. The arrangements of RC Adders shown in Fig. 5, helps us to reduce delay. Interestingly, 8x8 Vedic multiplier modules are implemented easily by using four 4x4 multiplier modules.

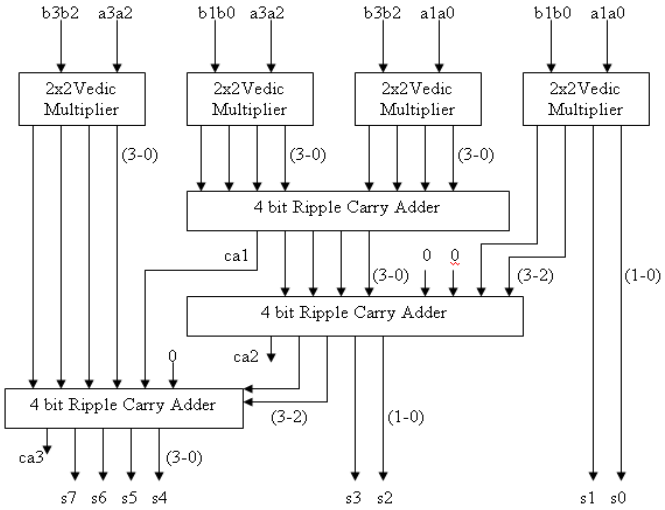

Fig. 5 Block Diagram of 4x4 bit Vedic Multiplier

C. Vedic Multiplier for 8x8 bit Module

The 8x8 bit Vedic multiplier module as shown in the block diagram in Fig. 6 can be easily implemented by using four 4x4 bit Vedic multiplier modules as discussed in the previous section. Let's analyze 8x8 multiplications, say A= $A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0$ and B= $B_7 B_6 B5B_4 B_3 B_2 B_1B_0$. The output line for the multiplication result will be of 16 bits as – $S_{15} S_{14} S_{13} S_{12} S_{11} S_{10} S_9 S_8 S_7 S_6S_5S_4 S_3 S_2 S_1 S_0$. Let's divide A and B into two parts, say the 8 bit multiplicand A can be decomposed into pair of 4 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL. The 16 bit product can be written as:

$$P = A \times B = (AH-AL) \times (BH-BL)$$
$$= AH \times BH + (AH \times BL + AL \times BH) + AL \times BL$$

Using the fundamental of Vedic multiplication, taking four bits at a time and using 4 bit multiplier block as discussed we can perform the multiplication. The outputs of 4x4 bit multipliers are added accordingly to obtain the final product. Here total three 8 bit Ripple-Carry Adders are required as shown in Fig. 6.

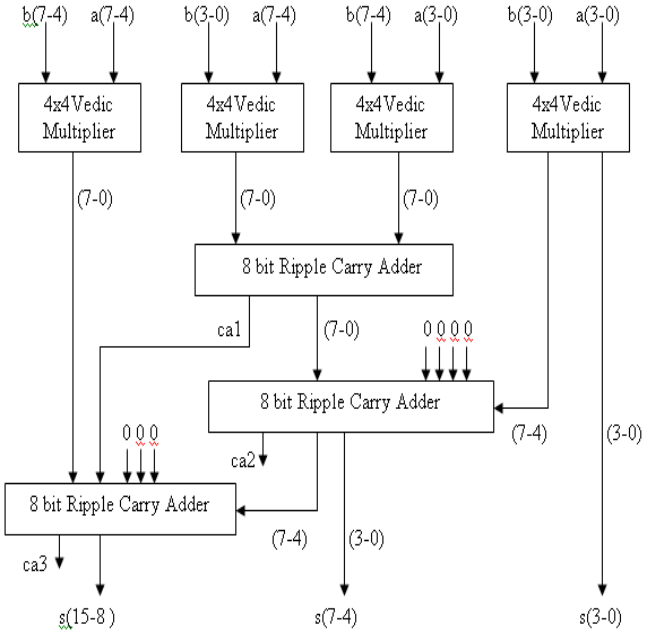

Fig. 6 Block Diagram of 8x8 bit Vedic Multiplier

D. Generalized Algorithm for N x N bit Vedic Multiplier

We can generalize the method as discussed in the previous sections for any number of bits in input. Let, the multiplication of two N-bit binary numbers (where N = 1, 2, 3…N, must be in the form of 2^N) *A* and *B* where A = A_N.....$A_3 A_2 A_1$ and B = B_N….$B_3 B_2 B_1$. The final multiplication result will be of (N + N) bits as S = $S_{(N+N)}$....$S_3 S_2 S_1$.

Step 1: Divide the multiplicand A and multiplier B into two equal parts, each consisting of [N to (N/2)+1] bits and [N/2 to 1] bits respectively, where first part indicates the MSB and other represents LSB.

Step 2: Represent the parts of A as A_M and A_L, and parts of B as B_M and B_L. Now represent A and B as A_M A_L and B_M B_L respectively.

Step 3: For A X B, we have general format as shown in Fig.

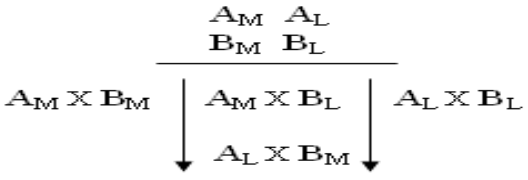

Fig. 7 General Representation for

Vedic Multiplication

Step 4: The individual multiplications product can be obtained by the partitioning method and applying the basic building blocks.

By adopting the above generalized algorithm we can implement Vedic Multiplier for any number of bits say 16, 32, 64, and so on, as per the requirement. Therefore, it could be possible to implement this Vedic multiplier in the ALU (Arithmetic Logic Unit) which will reduce the computational speed drastically & hence improves the processors efficiency.

IV. IMPLEMENTATION IN XILINX 12.1

In this work, 8x8 bit Vedic multiplier is designed in VHDL (Very High Speed Integrated Circuits Hardware Description Language). Logic synthesis and simulation was done using EDA (Electronic Design Automation) tool in XilinxISE12.1i - Project Navigator and ISim simulator integrated in the Xilinx package. The performance of circuit is evaluated on the Xilinx device family Spartan3, package tq144 and speed grade -5.

The RTL schematic of 8x8 bit Vedic multiplier "vedic_multi_struct8x8" comprises of four 4x4 bit Vedic multiplier "vedic_multi_struct4x4_1" - vm1, vm2, vm3, vm4 and three 7-bit Ripple Carry Adder "rc_adder_8" - r1, r2, r3 as shown in Fig. 8 while the simulation results obtained are shown in Fig. 9 for verification. In behavioral simulation we have tested for the following input bits: -

a) For 8x8 bit Vedic multiplier input, the multiplier a="00000101" (decimal number system 5) and multiplicand b="00000110" (decimal number system 6) and we get 16-bit output1= "0000000000011110" (decimal number system 30).

b) Again, we have multiplier a=00001000" (decimal number system 8) and multiplicand b="00000110" (decimal number system 3) with 16-bit output1="0000000000011000" (decimal number system 24).

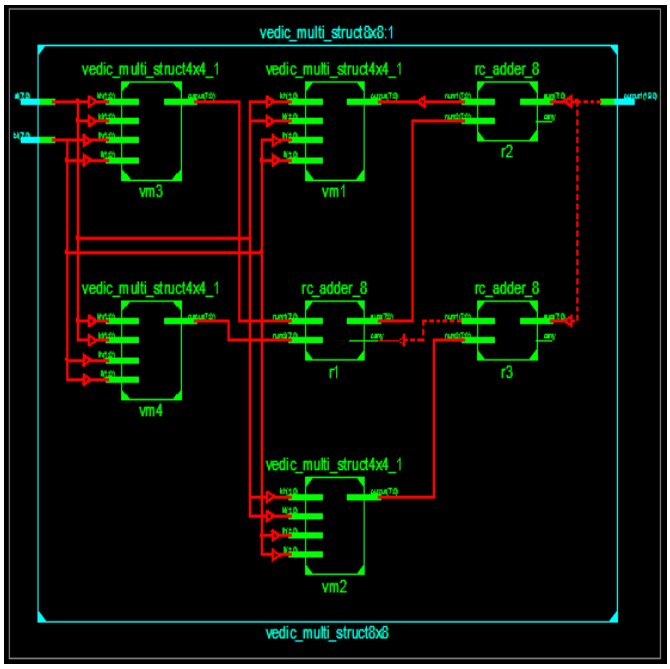

Fig. 8 RTL schematic of 8x8 bit Vedic Multiplier

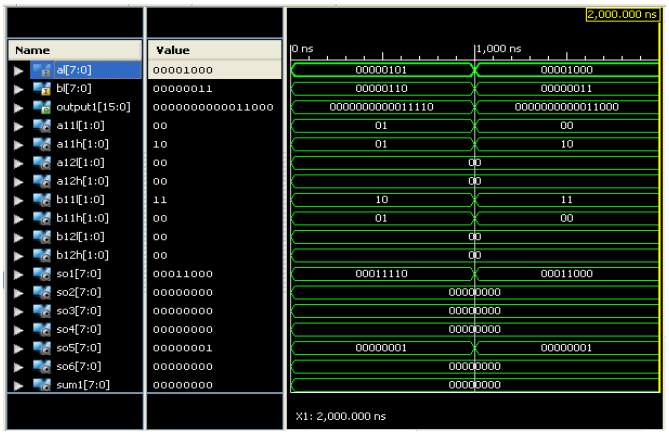

Fig. 9 Simulation Result of 8x8 bit Vedic Multiplier (5x6=30 & 8x3=24)

V. RESULT AND DISCUSSION

The synthesis result obtained from proposed Vedic multiplier is faster than Array and Booth multiplier. The device utilization summary of 8x8 bit Vedic multiplier for Xilinx, Spartan family is shown below:

Device Utilization Summary:

Selected Device:	3s50at q144-5		
Number of Slices:	95 out of	704	13%
Number of 4 input LUTs:	166 out of	1408	11%
Number of IOs:	32		
Number of bonded IOBs:	32 out of	108	29%

Table 1 shows the comparison of 8x8 bit Conventional multipliers with Vedic multiplier (ours) in terms of computational path delay in nanoseconds (ns). The path delay for 8x8 bit Array and Booth multipliers have been taken from S.S. Kerur et al. [11]. The timing result shows that Vedic multiplier has the greatest advantage as compared to other multipliers in terms of execution time.

Table 1 Comparison of 8x8 bit Multipliers (in ns)

Device: Spartan xc3s50a-5-tq144	Array Multiplier	Booth Multiplier	Vedic Multiplier
Path Delay	32.010 ns	29.549 ns	21.679 ns

VI. CONCLUSION

This paper presents a highly efficient method of multiplication – "Urdhva Tiryakbhyam Sutra" based on Vedic mathematics. It gives us method for hierarchical multiplier design and clearly indicates the computational advantages offered by Vedic methods. The computational path delay for proposed 8x8 bit Vedic multiplier is found to be 21.679 ns. Hence our motivation to reduce delay is finely fulfilled. Therefore, we observed that the Vedic multiplier is much more efficient than Array and Booth multiplier in terms of execution time (speed). An awareness of Vedic mathematics can be effectively increased if it is included in engineering education. In future, all the major universities may set up appropriate research centers to promote research works in Vedic mathematics.

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