A Review On Power Optimized TPG Using LP-LFSR For Low Power BIST

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***Abstract*— The main challenging areas in VLSI are performance, cost, and power dissipation. The demand for portable computing devices and communications system are increasing rapidly. These applications require low power dissipation VLSI circuits. The power dissipation during test mode is 200% more than in normal mode. This research article proposed a logic BIST using low power linear feedback shift register (LFSR) to generate low power test patterns. The designed architecture is programmed using VHDL and simulated using free active HDL tool. The experimental results demonstrate significant power reduction by low power TPG than compared to standard LFSR.**

Index Terms— Low power, Test Pattern Generation, Linear Feedback Shift Register, Logic Built in Self Test, DUT.

I. INTRODUCTION

POWER dissipation is a challenging problem for today's system-on-chips (SoC s) design and test. In general, the power dissipation of a system in test mode is more than in normal mode. Four reasons are blamed for power increase during test:
1. High-switching activity due to nature of test patterns,
2. Parallel activation of internal cores during test,
3. Power consumed by extra design-for-test (DFT) circuitry, and
4. Low correlation among test vectors.

This extra power consumption (average or peak) can create problems such as instantaneous power surge that cause circuit damage, formation of hot spots, difficulty in performance verification, and reduction of the product yield and lifetime. Solutions that are commonly applied to alleviate the excessive power problem during test include reducing frequency and test partitioning/scheduling to avoid hot spots. The former disrupts at-speed test philosophy and the latter may significantly increase the time. Built-In Self-Test (BIST) is a DFT methodology that aim sat detecting faulty components in a system by incorporating the test logic on chip .In BIST, a linear feedback shift register (LFSR)generates pseudorandom test patterns for primary inputs (for a combinational circuit) or scan chain inputs (for a sequential circuit).

The presented work proposes a low power Test Pattern Generator (TPG) to reduce the dynamic power consumed by Circuit under Test (CUT). The proposed design is programmed using VHDL language and simulated using free EDA tool or Active HDL tool. The design technique increases the correlation between successive test patterns to slenderize switching activity in Circuit under Test (CUT) which in turn decreases overall dynamic power consumption of CUT during test mode.

II. LITERATURE REVIEW

1] Sabir Hussain, K Padma Priya
"Test Pattern Generator (TPG) for Low Power Logic Built In Self Test (BIST)"
Author presented a Low Power LFSR architecture for Logic Built In Self Test. This is general and can be applied to almost all Test Pattern Generators. There method is based on swapping the adjacent bit pairs depending on the status of the last bit value. A considerable amount i.e. 27.48% of dynamic power saving was achieved with the help of this technique. After adding it with static (or leakage) power, got the net power and the net power saving was 25.11%.

2] Praveen Kasunde, Dr. K B ShivaKumar, Dr. M Z Kurian
"Improved Design of Low Power TPG Using LPLFSR"
A low power test pattern generator has been proposed which consists of a modified low power linear feedback shift register (LP-LFSR). The sequence generated from LPLFSR is Ex-ORed with the single input changing sequences generated from gray code generator, which effectively reduces the switching activities between the test patterns. Thus, the proposed method reduces the power consumption during testing mode with minimum number of switching activities using LP-LFSR instead of conventional LFSR.

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3] V.Kirthi1, Dr.G.Mamatha Samson
"Design of BIST with Low Power Test Pattern Generator"
Author presented a low power Test Pattern Generator has been incorporated in BIST developed for Vedic multiplier. The switching activities are reduced in the test pattern generation. Fault coverage is increased by the maximum number of clock cycles of the binary counter. The power consumption of different test pattern generation techniques has been found out and compared with the latest method. BIST is implemented for low power test pattern generator i.e, Vedic multiplier in the latest method. It is observed that the power consumption is reduced along with increased fault coverage when compared to other implementations.

4] Annie Chandra. D1,Thatchayani. K
" Power Reduction in TPG Based Built- in Self-Test(BIST) using LP/BS-LFSR on FPGA".
A low power test pattern generator has been proposed which consists of a modified low power linear feedback shift register (LP-LFSR).The test pattern generated from the LP-LFSR is EX-Ored single input changing sequence generated from the gray code generator, which reduces the switching activities. Thus ,the proposed method reduces the power dissipation during the test mode with minimum switching activity using LP/BSLFSR instead of normal LFSR. It is concluded that low power LFSR is very much useful for power consumption.

5] R. Vara PrasadaRao, N. Anjaneya Varaprasad, G. Sudhakar Babu, C. Murali Mohan
"Power Optimization of Linear Feedback Shift Register (LFSR) for Low Power BIST implemented in HDL".
Low power LFSR is very useful for BIST implementation in which the CUT may be Combinational, sequential and memory circuits. Using low power LFSR technique we can further decrease the power in BIST implementation.

III. PREVIOUS WORK

There has been various low power approaches proposed to solve the problem of power dissipation during the testing. One method is to use Random Single Input Change (RISC) test generation, which is used to generate low power test pattern. In this method, power consumption is reduced but at the additional cost is between 19% to 13%. In the second method it targets the average power consumption during normal circuit operations; they do not concern the average power consumption during test.

IV. PROPOSED WORK

In the proposed approach, an LFSR act as the LPLFSR that produces the modified test vectors to minimize the switching activity and consumes less power as compared to the normal LFSR .For low power BIST circuit partitioning suitable method to reducing the power. This approach consists in partitioning the original circuit into structural sub circuits so that each sub-circuits can be successively tested through different BIST session. The idea behind the use of such a low power TPG is to reduce the number of transition on primary inputs at each clock cycle of the test session, hence it reduces the total switching activity generated in the DUT.

A] Proposed system architecture

A typical BIST architecture consists of a test pattern generator (TPG),usually implemented as a linear feedback shift register(LFSR), MUX, DUT, BIST controller unit, comparator and ROM. The BIST architecture and its components are given below.

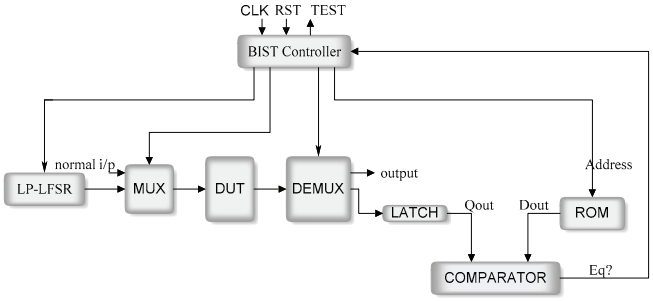

Figure1: Proposed BIST Architecture

B] Methodology

i) Hardware Test Pattern Generator(LP-LFSR): This module generates the test patterns required to sensitize the faults and propagate the effect to the outputs (of the DUT). As the test pattern generator is a circuit (not equipment) its area is limited. Instead, the test pattern generator is basically a type of register which generates random patterns which act as test patterns. The main emphasis of the register design is to have low area yet generate as many different patterns (from 0 to 2n, if there are n flip-flops in the register) as possible.

ii) Input Multiplexer: This multiplexer is to allow normal inputs to the circuit when it is operational and test inputs from the pattern generator when BIST is executed. The control input of the multiplexer is fed by a central test controller.

iii) Read Only Memory (ROM): Stores the test pattern that needs to be compared with the DUT response.

iv) Comparator*:* Hardware to compare compacted DUT response and the data which is already stored in the ROM.

v) Test Controller**:** Circuit to control the BIST. Whenever an IC is powered up (signal start BIST is made active) the test controller starts the BIST procedure. Once the test is over,

the status line is made high if fault is found. Following that, the controller connects normal inputs to the DUT via the multiplexer, thus making it ready for operation. Among the modules discussed above, the most important one is hardware test pattern generator (LFSR).

vi) DUT: DUT is referred to be the device under test i.e. the device which has to be tested. It may be a combinational circuit or a sequential circuit.

vii) DEMUX: Demultiplexer is allow the output of DUT to the comparator when it is in test mode. After the testing, if the DUT is working properly it can be used for the operation. The control input of the demultiplexer is fed by the central test controller.

viii) LATCH: Latch is used to hold the value of demultiplexer so that it cannot fluctuate.

A test controller provides all the necessary control signal to activate all the blocks. For test pattern generator we can use LP-LFSR as it uses less power. By selecting a control signal for mux, it selects the input from LP-LFSR for testing.The pattern from LP-LFSR is then fed to the DUT and according to the DUT, it perform the operation and output is given to the latch. Latch hold the output value for that particular clock cycle. The output from latch(Qout) and the data which is already stored in the ROM(Dout) get compared by using comparator.If the Qout is equal to the Dout then it informed to the controller and again next pattern is given to the DUT.In this way all the patterns get checked and if output is equal then we can say that DUT is working properly.If the DUT is not faulty then test pin becomes zero that means testing is done and we can apply normal input to the DUT.

C] PROPOSED LP-LFSR

Using Low power test pattern generator, a circuit's performance can be increased and switching activities can be reduced so that power dissipation will be reduced during test mode. We are going to implement a LP-LFSR techniques so that the power will reduce compared to previous works and also switching rate will be reduced in future.

In the proposed LP-LFSR, only one of the flip-flops in the LFSR register is enabled or activated during each shift operation, and as a result the low power LFSR according to the invention generates the same output bit sequence as a conventional LFSR. This lower flip-flop activity causes less power loss and, further, the longer the shift register and the smaller the feedback the more efficient is the low power LFSR.

Proposed LP-LFSR Architecture

Fig. shows the schematical block diagram of an embodiment of a proposed shift register (LFSR).

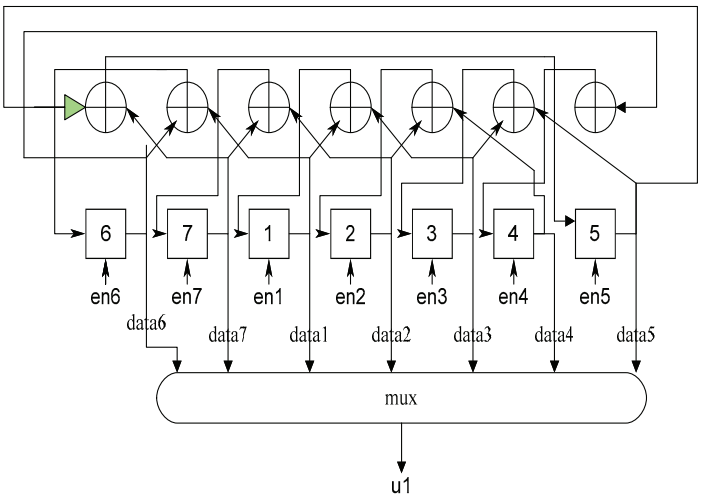

Figure2: Proposed LP-LFSR design

A low power linear feedback shift register according to the proposed architecture, using memory means such as flip-flops not consuming power when they are disabled. The register does not shift any bits but still generates the same sequence as a conventional linear feedback shift register.

The register comprises enabling means enabling a single current memory means at every shift operation, register stages, each comprising a low power memory means consuming a minimum of power when it is disabled, and feedback means of each stage. Each memory is connected to selection means, selecting at every shift operation the output terminal of a first subsequent memory means following the current memory means being enabled at the current shift operation.

CONCLUSION

We are going to implement all the blocks as discussed in the methodology. As discussed earlier, TPG which is designed from LP-LFSR decreases the power of BIST. The TPG is modified according to the various DUTS. The proposed Test Pattern Generator (TPG) will be designed and implemented using Active HDL tools.

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