KREST TECHNOLOGIES

arrow the aim

An ISO 9001 : 2000 Certified

VLSI PROJECT LIST (VHDL/Verilog)

S.No.	PROJECT TITLES	VHDL
1	An Efficient Implementation of Floating Point Multiplier	VHDL
2	An Efficient Architecture for 3-D Discrete Wavelet Transform. (Verilog)	Verilog
3	A Spurious-Power Suppression Technique for Multimedia/DSP Applications(Verilog)	Verilog
4	Design of On-Chip Bus with OCP Interface. (VHDL)	VHDL
5	DDR3 based lookup circuit for high-performance network processing. (Verilog)	Verilog
6	Multiplication Acceleration Through Twin Precision(VHDL)	VHDL
7	Implementation of FFT/IFFT Blocks for OFDM(VHDL)	VHDL
8	A Very fast and low power Carry select adder Circuit	Verilog
9	Implementation of UART Serial communication module based on VHDL	VHDL
10	RCEAT for Radio Frequency Identification (RFID) UHF Tag(Verilog)	Verilog
11	DA-based DCT core with an error-compensated adder-tree (ECAT) VHDL	VHDL
12	Low power ALU Design By Ancient Mathematics	VHDL
13	Efficient FPGA implementation of convolution	VHDL
14	Implementation of Carry Tree Adders using Verilog	Verilog
15	Implementation of Self-motivated Arbitration Scheme for the multi-layer AHB-Bus Matrix(Verilog)	Verilog
16	Self-Immunity Technique to Improve Register File Integrity against Soft Errors (Verilog)	Verilog
17	Implementation Of Hamming Code Using Verilog HDL	Verilog
18	Design of Parallel Multiplier Based on Radix-2 Modified Booth Algorithm (Verilog)	Verilog
19	Design and Implementation of Adaptive Viterbi Decoder (Verilog)	Verilog

20	High Performance Complex Number Multiplier Using Booth-Wallace Algorithm	VHDL
21	Design Of JPEG Image Compression Standard(Verilog)	Verilog
22	Design of an Bus Bridge between OCP and AHB Protocol (VHDL)	VHDL
23	Design of 16 Point Radix-4 FFT (Fast Fourier Transform) Algorithm(Verilog)	Verilog
24	Design of an AMBA-Advanced High performance Bus (AHB) Protocol IP Block(VHDL)	VHDL
25	Design of 32bit RISC PROCESSOR(VHDL)	VHDL
26	VMFU Design Using Spurious Power Suppression Technique	Verilog
27	Design of 16-bit QPSK	Verilog
28	Design of 64-bit QAM	Verilog
29	High Speed VLSI architecture for General Linear Feedback Shift Registers	Verilog
30	Implementation of High speed DDRSDRAM Controller	VHDL
31	Implementation of Guessing Game using VHDL	VHDL
32	Implementation of Traffic light controller using VHDL	VHDL
33	Implementation of DWT using(5,3) Lifting Scheme	Verilog
34	Design of Radix-2 Butterfly Processor to Prevent Overflow in the Arithmetic	VHDL
35	Design and Implementation of Systollic array Architecture for DWT	Verilog